HARDWARE OPEN SYSTEMS TECHNOLOGIES

Hardware Open Systems Technologies OpenVPX Core Technology Tier 2 Standard

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1 Overview

1.1 Objective

The Tier 2 Hardware Open System Technologies (HOST) OpenVPX Core Technology Standard applies OpenVPX embedded computing technologies to the HOST Tier 1 Standard architecture. This document introduces the application of OpenVPX as a Core Technology Standard, defines the conventions and conformance standards used in the document, and defines specific requirements of this Core Technology Standard. The Tier 2 Core Technology's Chassis Management is implemented using a subset of ANSI/VITA 46.11 and the associated Intelligent Platform Management Interface (IPMI) standard. This does not prohibit an implementation from using additional ANSI/VITA 46.11 and IPMI features that are not specifically required by this standard. This standard is intended to be backward compatible to these technologies. These VPX technologies are further supplemented by the addition of HOST specific requirements in order to establish stronger boundaries and communication standardization for chassis-wide solutions.

1.2 HOST OpenVPX Core Technology

The HOST OpenVPX Core Technology Standard defines technical requirements applying OpenVPX embedded computing technologies to the HOST Architecture. HOST Tier 2 standards are *Platform* agnostic and so this standard does not incorporate specific requirements of *Target Systems*. The goals of this HOST Core Technology Standard are to:

- Apply OpenVPX embedded computing technologies and leverage ANSI/VITA 46.11 for chassis management to define target-system agnostic requirements
- Facilitate OpenVPX computing hardware interoperability and reuse
- Facilitate the extensive use of OpenVPX *Commercial-Off-the-Shelf* (COTS) components
- Use IPMI and HOST-specific messages to complete the definition of the chassis management messaging protocol
- Enable the derivation of HOST Tier 3 component specifications from the combination of the HOST Tier 1 Standard, HOST Tier 2 Standard, and Target System requirements

Throughout the document, the standard is referred to interchangeably by the following terms: "HOST Tier 2 Standard," "Tier 2 HOST Standard," and "Tier 2 Core Technology Standard."

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1.3 **Referenced Documents**

ANSI/VITA 42.0-2008 (R2014), Switched Mezzanine Card (XMC)

ANSI/VITA 42.3-2006 (R2014), XMC PCI Express Protocol Layer Standard

ANSI/VITA 46.0-2013 (R2013), VPX Base Standard

ANSI/VITA 46.6-2013, Gigabit Ethernet Control Plane on VPX

ANSI/VITA 46.7-2012, Ethernet on VPX Fabric Connector

ANSI/VITA 46.9-2010, PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard

ANSI/VITA 46.11-2015, System Management on VPX

ANSI/VITA 47-2005 Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard

ANSI/VITA 48.2-2010 Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to ANSI/VITA VPX

ANSI/VITA 62.0-2012, Modular Power Supply Standard

ANSI/VITA 65.0-2010 (R2012), OpenVPX

ANSI/VITA 66.0-2016, Optical Interconnect on VPX – Base Standard

ANSI/VITA 67.0-2012, Coaxial Interconnect on VPX - Base Standard

ANSI/VITA 67.2-2012, Coaxial Interconnect on VPX, 8 Position SMPM Configuration

IEEE 802.3-2012 (December 28, 2012), IEEE Standard for Ethernet

IEEE 1386.1-2001 (June 14, 2001), IEEE Standard Physical and Environmental Layers for PCI Mezzanine

Intelligent Platform Management Interface (IPMI) Specification Version 2.0, Revision 1.1, dated 01 October 2013

IPC-J-001F (July 2014), Requirements for Soldered Electrical and Electronic Assemblies

IPC-CC-830B with Amendment 1 (October 2008), Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPMI Platform Management FRU Information Storage Definition Version 1.0, Revision 1.2, dated 28 February 2013

United States Computer Emergency Readiness Team (US-CERT) Alert (TA13-207A) “Risks of Using the Intelligent Platform Management Interface (IPMI),” dated 26 July 2013

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2 Implementation

This Tier 2 HOST Standard governs the implementation of HOST conformant systems utilizing the ANSI/VITA 65.0 OpenVPX System Specification and related embedded computing standards. More specifically, this Tier 2 Architecture defines the implementation of the following HOST Architecture elements with OpenVPX as the core technology for Hardware. ANSI/VITA 46.11 and Intelligent Platform Management Interface (IPMI) standards are leveraged for hardware management.

2.1 HOST Management

HOST Management (HOST-MGMT) establishes an autonomous subsystem that provides application independent hardware management and monitoring capabilities for the module, chassis, and system domains. The inclusion of HOST-MGMT in the HOST Standard is intended to ensure completeness in the specification of all hardware, software, and firmware necessary to implement and standardize the management functions and interfaces. This Tier 2 HOST Standard leverages ANSI/VITA 46.11 and IPMI standards to define the required data exchanges and hardware provisions for a HOST-MGMT solution.

2.1.1 Logical Control Elements

HOST-MGMT implements logical control elements known as the *Manager*, *Participants*, and *Remote Participants* that are used in the context of a communication protocol to coordinate messaging between *HOST Modules* and to perform general management duties. In many regards, these terms are synonymous with HOST-MGMT in that they represent HOST software or firmware implemented for purposes of meeting the intent of the management requirements defined by the HOST Standard. Applying the labels Manager, Participant, and Remote Participant highlights the logical role of these entities and reinforces the ideas of HOST Module representation and command/control relationships that are fundamental to HOST-MGMT. This Tier 2 HOST Standard uses ANSI/VITA 46.11 defined management controllers to define the HOST logical control elements.

2.1.2 Inventory Information Records and Event Logs

HOST-MGMT Event Logs and HOST-MGMT Inventory Information Records are intended to contain the information necessary to uniquely identify hardware components and to capture events that identify and isolate hardware failures and anomalies at the module level. The logs and records adhere to the overarching philosophy of the module as the atomic unit with aggregate information available at the chassis level. Memory allocation and memory access considerations need to be addressed in hardware requirements to account for these features. This Tier 2 HOST Standard uses ANSI/VITA 46.11 defined structures to define the HOST Event Logs and Inventory Information Records.

2.1.3 Manager/Participant Protocol

HOST-MGMT defines communication between the Manager and Participants using a standardized means of data exchange known as *Manager/Participant Protocol* (MPP). The selection of an open, standardized, non-proprietary protocol ensures interoperability between HOST Modules and guarantees support for a fundamental set of functionality. This Tier 2 HOST Standard defines the data exchanges and their structures used in the MPP protocol using ANSI/VITA 46.11 and IPMI standards. MPP consists of Addressing structure and ANSI/VITA 46.11 messages which are implemented in designing individual modules inside of the chassis compartment. The Addressing structure is designed using ANSI/VITA 46.11 for all the MPP messages. The unique address is generated per VPX Hardware Address, *Intelligent Platform Management Bus* (IPMB) Address, Physical Address, and *Field Replaceable Unit* (FRU) Device ID.

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2.2 Hardware Implementation

This Tier 2 HOST Standard standardizes hardware components and their interfaces to facilitate interoperability between the components residing in a chassis.

2.2.1 HOST Components

HOST Components are divided into four main categories: Modules, External Interfaces, Transmission Interfaces, and the Enclosure.

2.2.1.1 HOST Modules

HOST Modules are implemented as a *Plug-In* or as *Mezzanine Modules*.

HOST Plug-In Modules are implemented using ANSI/VITA 65.0/ANSI/VITA 48.2 Conduction-Cooled Payload and Switch Modules, and ANSI/VITA 62.0 Power Supplies.

HOST Mezzanine Modules are implemented using ANSI/VITA 42.0/42.3 Switched Mezzanine Cards (XMC) Standard and IEEE 1385-2001 PCI Mezzanine Cards (PMC).

2.2.1.2 Transmission Interface

Transmission Interfaces are responsible for the Logical and Physical connectivity within the system. For this Tier 2 core technology, Transmission Interfaces are implemented utilizing backplanes composed of HOST-specific and ANSI/VITA 65.0 design elements.

2.2.1.3 HOST Enclosure

The *HOST Enclosure* is implemented utilizing ANSI/VITA 48.2 and ARINC 404 1-ATR enclosure design elements.

2.3 Resource Implementation

Although this Tier 2 HOST Standard is based primarily upon the use of OpenVPX as the core technology, it will further define requirements for making OpenVPX components HOST conformant. Therefore, a component that is OpenVPX conformant is not necessarily HOST conformant.

FIGURE 2-1 shows an example of how the resources could be implemented on different HOST Modules.

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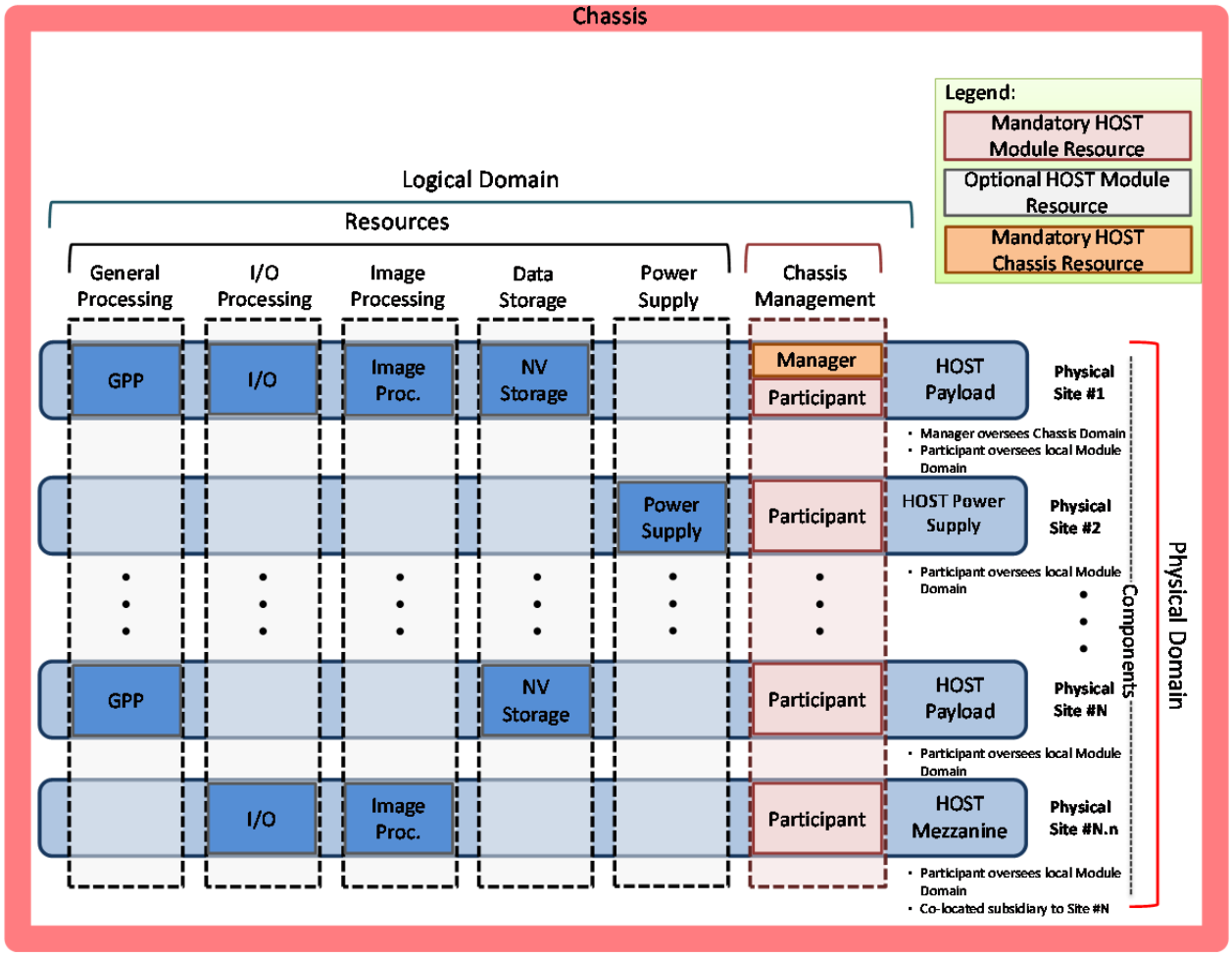

Figure 2-1 – Resource Implementation Example

In FIGURE 2-1 the HOST Payload Module is based on an ANSI/VITA 65.0 Plug-In Module, the HOST Mezzanine could be either a PMC or XMC module, and the HOST Power Supply is based on an ANSI/VITA 62.0 Power Supply Plug-In Module. (Note: Terminology in this standard follows the ANSI/VITA standard where a mezzanine is interchangeably called a card or module.)

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3 Guidelines

3.1 Typography

The following typographical conventions are used throughout this document:

- *Italics* – Indicates a term defined in the glossary or for emphasis (occurs on first instance).
- **Bold** – Indicates keywords and their terms (ex: “shall”, “should”, “may”) as defined in SECTION 3.2.
- SMALL CAPS - Cross-reference to another section, figure, or table in this document.

3.2 Keywords

To avoid confusion and to make very clear what the requirements for conformance are, many of the paragraphs in this standard are labeled with keywords that indicate the type of information they contain. These keywords are listed below:

• Rule
• Recommendation
• Permission
• Observation

Any text not labeled with one of these keywords is to be interpreted as descriptive in nature. These will be written in either a descriptive or a narrative style.

Keywords are reserved for specific use as defined in subsequent sections. When a reference to a section or paragraph from an external source is included in a Keyword statement, it is intended that it also contains all lower level sections and paragraphs.

3.2.1 Rule

Compliance with Rules is mandatory. Rules always include the term “**shall**.” Rules are expressed in some combination of text, figures, tables, or drawings. All Rules will be followed to ensure compatibility between board and Backplane designs. The word “**shall**” is reserved exclusively for stating Rules in this standard and is not used for any other purpose.

3.2.2 Recommendation

Compliance with Recommendations is optional. Recommendations always include the term “**should**.” Recommendations are used to convey implementation advice based on the community’s collective knowledge base. Recommendations found in this standard are based on experience and are provided to designers to reduce their learning curve. The word “**should**” is reserved exclusively for stating Recommendations in this standard and is not used for any other purpose.

3.2.3 Permission

Compliance with Permissions is optional. Permissions always include the term “**may**.” In some cases, a Rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the Rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable. The word “**may**” is reserved exclusively for stating Permissions in this standard and is not used for any other purpose.

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3.2.4 **Observation**

Observations do not offer any specific advice. They are provided to enhance comprehension and usually follow naturally from what has just been discussed. They spell out the implications of certain Rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain Rules so that the reader understands the spirit of the Rule.

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4 HOST Conformance

4.1 HOST Conformance

Defining conformance and creating a method for verifying and certifying HOST products is vital to establishing an effective standard. Certification provides formal recognition of conformance to a HOST standard or specification. Without the associated conformance criteria and processes, there is no assurance that a supplier has developed or implemented products or solutions according to the approved HOST Technical Standards and Specifications. Verification provides evidence of conformance to a Technical Standard or specification, which allows:

- Buyers to specify and successfully procure hardware from vendors who provide solutions that conform to the HOST Specifications and Standards.
- System Integrators to make and substantiate clear claims of conformance to HOST Specifications and/or Standards.
- Hardware component suppliers to make and substantiate clear claims of conformance to HOST Specifications.

The government will establish conformance criteria and define an associated Conformance Program for the HOST Tier 3 Specifications and HOST Components.

The Conformance assessment is intended to certify compliance with HOST requirements and is not intended to insure a component or system will function as intended in its final application. Conformance assessment is not meant to assist with or replace developmental or operational test.

4.2 HOST Conformance Program

The HOST Conformance Program will have two primary functions:

1) Verification that a newly developed or revised Tier 3 Specification complies with the requirements of the applicable HOST Tier 2 Standard.
2) Verification that a hardware component complies with the requirements of the applicable HOST Tier 3 Specification.

4.2.1 HOST Conformance Program Terminology

HOST Conformance is defined as 100 percent compliance with all HOST requirements.

HOST Verification is the act of determining the conformance of a HOST product to the applicable HOST technical standard or specification requirements. The applicable Tier 2 Standards and Tier 3 Specification will have associated matrices that recommend or specify a verification method for each rule. Verification will be carried out by the agency responsible for developing the HOST product being verified. Results and artifacts of the verification will be submitted to a Verification Authority (VA). The VA will review the verification results and artifacts to make a determination on whether the verification process was sufficiently correct and complete to show conformance to the next higher level specification or standard.

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Publication is the process of entering a HOST Specification into a registry. Specifications residing in the registry will be available to outside Government agencies and commercial companies. Distribution of the published document will be controlled by the distribution statement on the cover page.

HOST Registration is the process of listing Certified HOST Tier 3 Specifications and Components in a public listing known as the HOST Registry.

4.2.2 HOST OpenVPX Verification Methods Document

Detailed verification method information required for Tier 3 Specifications that conform to the requirements of this document are detailed in a companion document to this standard titled: HOST OpenVPX Verification Methods (HOVM).

The HOVM contains a Conformance Verification and Applicability Matrix (CVAM). The CVAM will include entries for all HOST Tier 2 requirements and identify, at a minimum, the following details for each Tier 2 rule: requirement ID, applicability to the specific types of components identified in the Tier 2 Standard, recommended verification method for the requirement, and additional information as necessary. The HOVM also defines the types of documentation that are required for verification of a Tier 3 Specification.

4.2.3 HOST Tier 3 Specification Conformance

Tier 3 Specifications will be verified to show conformance to this Tier 2 Standard. The agency authoring the Tier 3 Specification will perform and document a requirements trace to show that all applicable rules of this document have been flowed down to the Tier 3 Specification. In addition a check will be made to verify that the Tier 3 Specification's Conformance Verification Matrix (CVM) covers all of the requirements identified in the Tier 3 Specification. The Tier 3 CVM will be checked to verify that it lists the appropriate verification methodology for each requirement per the CVAM contained in the HOVM. The submitting agency will provide the results of their verification efforts and supporting documentation to be reviewed by the VA. Upon successful completion of the HOST Tier 3 conformance process, the Tier 3 Specification will be published.

4.2.4 HOST Component Conformance

Components will be verified to show conformance to the applicable HOST Tier 3 Specification. Verification methods for component requirements will be identified in a CVM included in the Tier 3 Specification. The submitting agency will perform verification of the developed product to show conformance to the Tier 3 Specification. The submitting agency will provide the results of their verification efforts and supporting documentation to be reviewed by the VA. Upon successful completion of the HOST conformance process and review by the VA, the component data will be entered into the HOST Registry.

4.2.5 Conformance Verification Matrix

The Tier 3 Specification will include a CVM. The purpose of the CVM is to specify the required verification method for each Tier 3 Specification requirement. The CVM will include an entry for each requirement contained in the Tier 3. The CVM will identify whether or not a requirement traces to a HOST Tier 2 Standard requirement. In addition, the CVM will include the required verification method, an indication on whether the requirement was derived from a HOST Tier 2 Standard or system performance requirement, associated HOST Tier 2 requirement when applicable, and additional information as necessary for each Tier 3 requirement.

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T2-RUL-0001: A HOST Tier 3 Specification conforming to this standard **shall** include a CVM that includes an entry for each rule of this standard.

T2-RUL-0002: For each Tier 2 rule, the Tier 3 CVM **shall** indicate whether the rule is applicable to the type of component defined in the Tier 3 Specification (per the CVAM).

T2-RUL-0003: For each Tier 2 rule applicable to the type of component specified in the Tier 3, the Tier 3 CVM **shall** specify the required verification method in accordance with the CVAM included in the HOVM document.

T2-RUL-0004: For each Tier 2 rule applicable to the type of component specified in the Tier 3, the Tier 3 Specification **shall** identify the required artifacts and any additional information required for verification.

4.2.6 **Verification Methods**

HOST Component requirements will be based on one of the following conformance methods: *Inspection*, *Analysis*, *Demonstration*, or *Test*.

5 **Tier 2 Standard Requirements**

5.1 **HOST Module Requirements**

This HOST Tier 2 Core Technology Standard implements HOST Modules as 6U and 3U OpenVPX Plug-In Modules, ANSI/VITA 62.0 Power Supply Plug-In Modules, and PMC/XMC Mezzanine Modules. HOST Plug-In Modules consist of HOST Payload Modules, HOST Switch Modules and HOST Power Supply Modules (PSM) that connect (plug-in) directly to the *HOST Backplane* component. HOST Payload Modules are used to implement the *General Processing Resource* (GPR), *I/O Processing Resource* (IOPR), *Image Processing Resource* (IPR) and *Data Storage Resource* (DSR) functional resources and/or act as carriers of HOST Mezzanine Modules. HOST Switch Modules provide *System Communications Transmission Interface* (SCTI) interconnection between HOST Payload Modules. HOST Power Supply Modules transform Platform power into system power for use by HOST Payload and Switch modules.

The hierarchy of rules for the various HOST Module types is shown in FIGURE 5-1.

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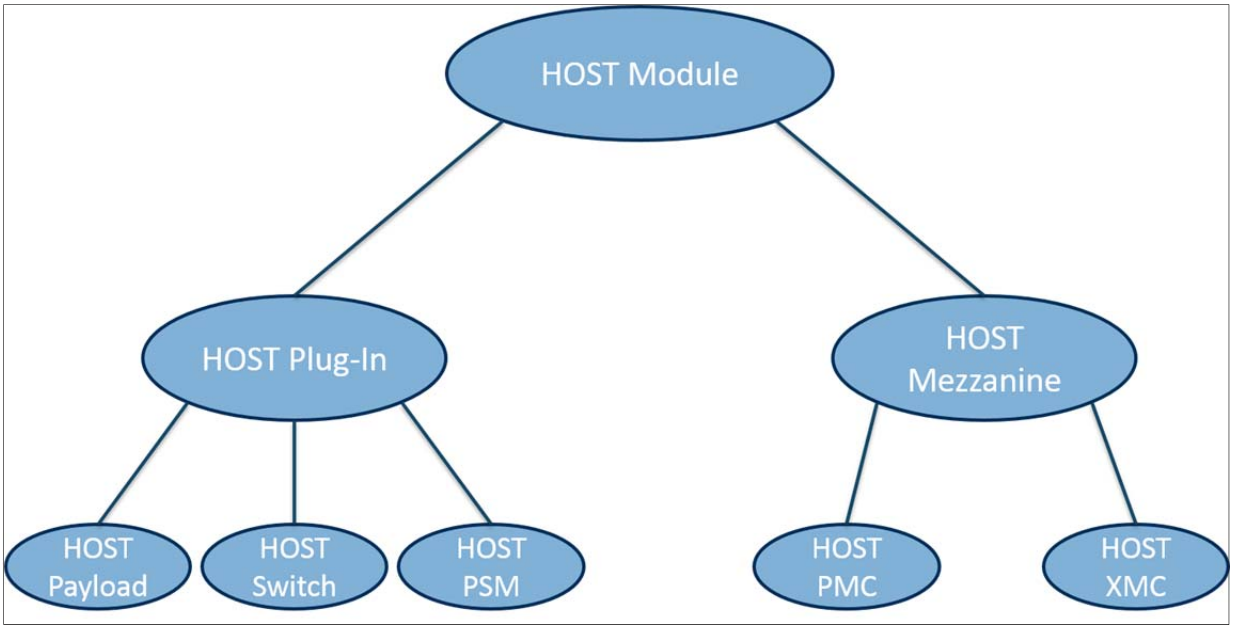

Figure 5-1 – HOST Module Rules Hierarchy

The module hierarchy clarifies which rules each module type must follow. For example, a HOST Switch must follow any rules levied on HOST Switches, HOST Plug-Ins, and HOST Modules; but a HOST Switch does not have to follow rules levied on HOST Payloads, HOST PSMs, or HOST Mezzanines.

T2-RUL-0010: For this Tier 2 Core Technology Standard a HOST Module **shall** be defined as a Payload Module, Switch Module, Power Supply Module, PMC Mezzanine Module, or a XMC Mezzanine Module.

T2-RUL-0011: Payload, Switch, and Power Supply Modules **shall** conform to the requirements of Plug-In Modules.

T2-RUL-0012: PMC and XMC Modules **shall** conform to the requirements of Mezzanine Modules.

T2-RUL-0020: A HOST Module **shall** conform to interface requirements of the *Chassis Management Transmission Interface* (CMTI) per SECTION 5.3.1.5.

T2-PER-0010: A HOST Module **may** utilize the *System I/O Transmission Interface* (SIOTI) per SECTION 5.3.1.3.

T2-RUL-0030: A HOST Module **shall** conform to the interface requirements of the *System Power Distribution Interface* (SPDI) per SECTION 5.3.1.6.

T2-RUL-0052: HOST Modules **shall** leave signals HOST defines as reserved unconnected.

T2-PER-0012: A HOST Module **may** have only a subset of the SPDI voltages defined within the OpenVPX Utility Plane as an input.

T2-RUL-0031: If a HOST Module uses only a subset of the SPDI voltages defined within the OpenVPX Utility Plane as an input, the HOST Module **shall** leave the pins meant for the unused voltages as Reserved.

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5.1.1 HOST Plug-In Module Requirements

T2-RUL-0053: Plug-In Modules **shall** follow ANSI/VITA 46.0, Rule 3-1 regarding safety ground.

T2-RUL-0054: Plug-In Modules **shall** follow ANSI/VITA 46.0, Rule 3-15 regarding dielectric separation.

T2-RUL-0057: Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, SECTION 4.8.9 3.3V_AUX.

T2-RUL-0058: Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, SECTION 4.8.11 SYSRESET*.

T2-RUL-0059: Plug-In Modules **shall** draw no more than 1 mA from VBAT per rule 4-56.1 of ANSI/VITA 46.0.

T2-RUL-0061: If implementing the 12V_AUX +/-, Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, SECTION 4.8.10 12V_AUX.

5.1.1.1 Payload Modules

5.1.1.1.1 Common 6U and 3U Payload Module Requirements

This Tier 2 HOST Standard utilizes one set of HOST-defined OpenVPX slot and *Module Profiles* for all HOST Payload Modules. The *Slot Profile* maps specific OpenVPX module connections to the HOST System Communications, System I/O, Chassis Management, and System Power Interfaces made available at the Backplane. The Module Profile specifies serial channel baud rates. HOST Payload Modules are a type of HOST Plug-In Module.

T2-RUL-0140: Payload Modules **shall** conform to the interface requirements of the SCTI per SECTION 5.3.1.2.

T2-RUL-0055: Payload Modules **shall** be designed to accommodate any combination of power supply power up and power down sequences without causing board failure.

T2-RUL-0056: Payload Modules **shall** follow the rules of ANSI/VITA 46.0, SECTION 4.8.3 System Controller.

T2-REC-0010: Single-ended user defined signals that require tight tolerances, precise values, very short rise times, and high current **should** be routed over the positive pin of the differential pair and the negative pin of the differential pair should be grounded. This is to prevent potential cross talk of the single-ended user defined signals.

T2-PER-0020: Payload Modules **may** draw power from the VBAT, battery backup power rail on the OpenVPX Utility Plane per ANSI/VITA 65.0, SECTION 3.2.2.

T2-OBS-0080: The SPDI supports the battery backup power rail per ANSI/VITA 65.0, SECTION 3.2.2 and ANSI/VITA 46.0, SECTION 4.9.2.

T2-OBS-0081: Refer to recommendations of ANSI/VITA 65.0, SECTION 3.2.4 on inrush (surge) current.

T2-RUL-0231: Payload Modules **shall** implement the Utility Plane requirements as defined in SECTION 5.3.1.5.1.1.

T2-RUL-0240: Payload Modules **shall** implement the requirements of ANSI/VITA 65.0, 6.3.3, (User Defined).

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T2-OBS-0150: The OpenVPX User Defined connections are part of the SIOTI as defined in SECTION 5.3.1.3.

5.1.1.1.1.1 Common Payload Module with Mezzanine Site Requirements

T2-RUL-0080: Payload Modules with PMC mezzanine sites **shall** conform to the carrier, termed host in IEEE 1386.1, board requirements of IEEE 1386.1.

T2-RUL-0090: Payload Modules with XMC mezzanine sites **shall** conform to the carrier board requirements of ANSI/VITA 42.0, XMC.

T2-OBS-0010: Compatibility with the PMC/XMC communications protocols is defined by the SCTI in SECTION 5.3.1.2.

T2-OBS-0020: Compatibility with the PMC/XMC power interfaces is defined by the SPDI in SECTION 5.3.1.6.

T2-OBS-0030: It is possible for a single mezzanine site to be compatible with both XMC and PMC mezzanine formats.

T2-OBS-0040: Mezzanine connector pinout requirements for Payload Modules with PMC Mezzanine sites are specified by IEEE Std. 1386.1-2001 SECTION 5.2.

T2-OBS-0050: Voltage keying requirements for Payload Modules with PMC Mezzanine sites are specified by IEEE Std. 1386.1-2001 SECTION 4.2.

T2-OBS-0060: Mezzanine connector pinout requirements for Payload Modules with XMC Mezzanine sites are specified by ANSI/VITA 42.0 SECTION 5-1.

T2-OBS-0070: It is possible for Payload Modules to be mezzanine carriers that do not natively contain any resources. In those cases, the Payload Module may only contain the bridges required to attach the PMC/XMC modules to the SCTI and CMTI.

T2-RUL-0100: Payload Module mezzanine sites configured to support a XMC Mezzanine **shall** implement the secondary XMC connector ground pins in accordance with ANSI/VITA 42.0 Table 5-4, Secondary XMC Connector Pin Definition.

5.1.1.1.2 6U Payload Module Requirements

T2-RUL-0070: 6U Payload Modules **shall** conform to the 6U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0051: 6U Payload Modules **shall** follow ANSI/VITA 65.0, SECTION 12.1.2 with regards to Power Voltages and System Management.

T2-OBS-0079: Refer to ANSI/VITA 65.0, Recommendation 12.1.1.2-1 regarding maximum module power draw.

T2-RUL-0180: 6U Payload Modules **shall** conform to the Slot Profile SLT6-PAY-4F1Q2U2T-HOST as shown in FIGURE 5-2.

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T2-RUL-0250: 6U Payload Modules **shall** conform to the Module Profile MOD6-PAY-4F1Q2U2T-HOST shown in TABLE 5-1 for the pipes that are implemented per SECTION 5.1.1.1.1.1.

5.1.1.1.2.1 6U Slot Profile, SLT6-PAY-4F1Q2U2T-HOST

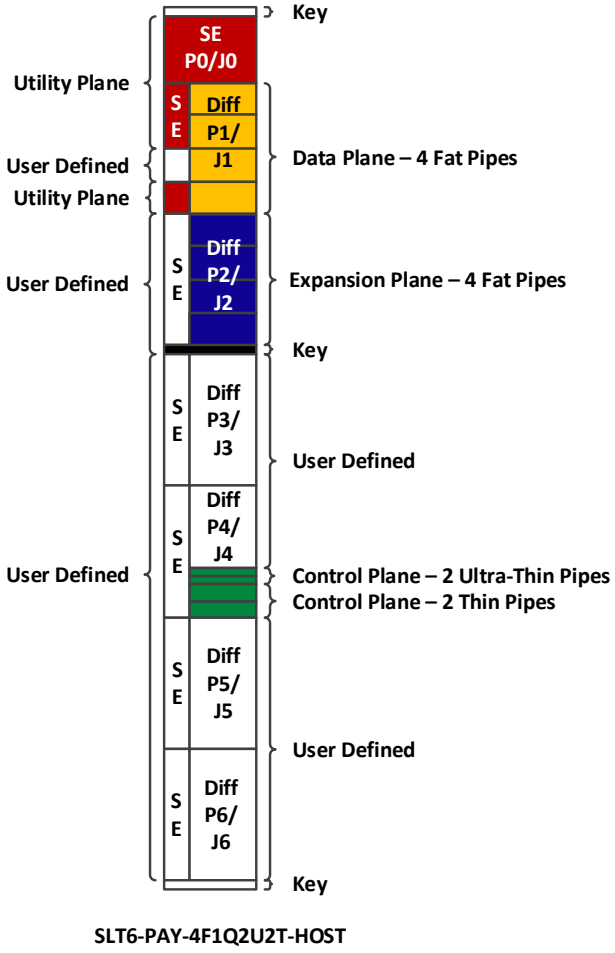

Figure 5-2 – HOST Payload Slot Profile, SLT6-PAY-4F1Q2U2T-HOST

T2-RUL-0190: If 6U Payload Modules implement the Data Plane, Payload Modules **shall** implement the first Data Plane fat pipe as defined by ANSI/VITA 65.0, section 10.2.1.3.

T2-PER-0030: 6U Payload Modules **may** implement all four Data Plane fat pipes as defined by ANSI/VITA 65.0, section 10.2.1.3.

T2-OBS-0100: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.3.1.2.

T2-RUL-0193: If 6U Payload Modules implement the Expansion Plane, Payload Modules **shall** implement the first Expansion Plane fat pipe as defined by ANSI/VITA 65.0, section 10.2.1.3.

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T2-PER-0031: 6U Payload Modules **may** implement all four Expansion Plane fat pipes as defined by ANSI/VITA 65.0, section 10.2.1.3.

T2-OBS-0101: The OpenVPX Expansion Plane is part of the SCTI as defined in SECTION 5.3.1.2.

T2-RUL-0191: If 6U Payload Modules implement the Control Plane ultra-thin pipes, Payload Modules **shall** implement the first Control Plane ultra-thin pipe as defined by ANSI/VITA 65.0, section 10.2.1.2.

T2-PER-0040: 6U Payload Modules **may** implement both Control Plane ultra-thin pipes as defined by ANSI/VITA 65.0, section 10.2.1.2.

T2-RUL-0192: If 6U Payload Modules implement the Control Plane thin pipes, Payload Modules **shall** implement the first Control Plane thin pipe as defined by ANSI/VITA 65.0, section 10.2.1.2.

T2-PER-0042: 6U Payload Modules **may** implement both Control Plane thin pipes as defined by ANSI/VITA 65.0, section 10.2.1.2.

T2-RUL-0200: If a 6U Payload Module implements the Control Plane thin pipes, a Payload Module **shall** use the Control Plane thin pipes exclusively for debug.

T2-OBS-0110: The OpenVPX Control Plane is part of the CMTI as defined in SECTION 5.3.1.5.

T2-OBS-0111: The UTPs of the OpenVPX Control Plane are also part of the SCTI as defined in SECTION 5.3.1.2.

T2-OBS-0120: Reserved signals cannot be utilized for any other purpose (such as user I/O).

5.1.1.1.2.2 6U Module Profile, MOD6-PAY-4F1Q2U2T-HOST

Table 5-1 – HOST Payload Module Profile, MOD6-PAY-4F1Q2U2T-HOST

Profile Name	Data Plane 4 FP				Expansion Plane 4FP				Control Plane 2 UTPs		Control Plane 2 TPs	
	DP01	DP02	DP03	DP04	DP04	DP04	DP04	DP04	CPutp 01	CPutp 02	CPtp 01	CPtp 02
MOD6-PAY-4F1Q2U2T-HOST	10GBase-KX4 Ethernet per ANSI/VITA 65.0 Section 5.1.5				PCIe per ANSI/VITA 65.0 section 5.3				1000BASE-KX or BX per ANSI/VITA 46.6		1000BASE-T per ANSI/VITA 65.0 section 5.1.1	

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T2-OBS-0153: The following ANSI/VITA 65.0 Module Profiles are compatible with MOD6-PAY-4F1Q2U2T-HOST:

- MOD6-PAY-4F1Q2U2T-12.2.1-7
- MOD6-PAY-4F1Q2U2T-12.2.1-8

T2-PER-0041: 6U Payload Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR Ethernet per clause 72 of IEEE 802.3. Note that it will still need to be able to support 10GBase-KX4.

T2-PER-0045: 6U Payload Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0062: 6U Payload Modules using 10GBASE-KR **shall** comply with clause 72 of IEEE 802.3.

T2-OBS-0151: If implementing 10GBASE-KR the pin mapping should still comply with ANSI/VITA 46.6 but ANSI/VITA 46.7, section 5 should be consulted for electrical requirements and channel compliance.

T2-OBS-0152: A specific version of PCIe is not called out in this profile to allow for future generations of PCIe.

5.1.1.1.2.3 6U Payload Module with Mezzanine Site Requirements

T2-RUL-0110: 6U Payload Module mezzanine sites configured to exclusively support a PMC Mezzanine **shall** conform to ANSI/VITA 46.9, section 5.1 regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0120: 6U Payload Module mezzanine sites configured to exclusively support a XMC Mezzanine **shall** conform to ANSI/VITA 46.9, section 5.4 regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0130: 6U Payload Module mezzanine sites configured to support both PMC and XMC Mezzanines **shall** conform to ANSI/VITA 46.9, section 5.2 regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

5.1.1.1.2.4 6U HOST Payload Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements

T2-PER-0046: 6U Payload Modules **may** replace the P6 connector with an ANSI/VITA 66.0 or ANSI/VITA 67.0 compliant blind mate connector.

T2-RUL-0131: If following Permission 0046, 6U Payload Modules **shall** only replace the P6 connector.

T2-PER-0047: 6U Payload Modules **may** replace the P5 and P6 connector with an ANSI/VITA 66.0 or ANSI/VITA 67.0 compliant blind mate connector.

T2-RUL-0132: If following Permission 0047, 6U Payload Modules **shall** exclusively replace the P5 and P6 connector.

T2-RUL-0134: 6U Payload Modules **shall** exclusively use blind mate Fiber Optic interconnects defined in ANSI/VITA 66.0 and its related dot standards for interfacing with fiber optic cables.

T2-RUL-0135: 6U Payload Modules using optical interconnects **shall** conform to the requirements of the chosen blind mate connector's respective ANSI/VITA 66.0 dot standard.

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T2-RUL-0136: 6U Payload Modules using optical interconnects **shall** use full width variants of the Fiber Optic blind mate connectors.

T2-RUL-0137: 6U Payload Modules using coaxial interconnects **shall** exclusively use the blind mate Coaxial interconnect defined in ANSI/VITA 67.2.

T2-RUL-0138: 6U Payload Modules using coaxial interconnects **shall** conform to the requirements of ANSI/VITA 67.2.

T2-RUL-0139: If a 6U Payload Module follows permission 0046 or permission 0047, a 6U Payload Module **shall** only use mezzanine site 1 which maps to P3 and P4.

5.1.1.1.3 3U Payload Module Requirements

T2-RUL-0142: 3U Payload Modules **shall** conform to the 3U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0141: 3U Payload Modules **shall** follow ANSI/VITA 65.0, section 16.1.2 with regards to Power Voltages and System Management.

T2-OBS-0154: Refer to ANSI/VITA 65.0, Recommendation 16.1.1.2-1 regarding maximum module power draw.

T2-RUL-0143: 3U Payload Modules **shall** conform to the Slot Profile SLT3-PAY-2F2U-HOST as shown in FIGURE 5-3.

T2-RUL-0144: 3U Payload Modules **shall** conform to one of the Module Profiles shown in TABLE 5-2 for the pipes that are implemented per SECTION 5.1.1.1.1.1.

5.1.1.1.3.1 3U Slot Profile, SLT3-PAY-2F2U-HOST

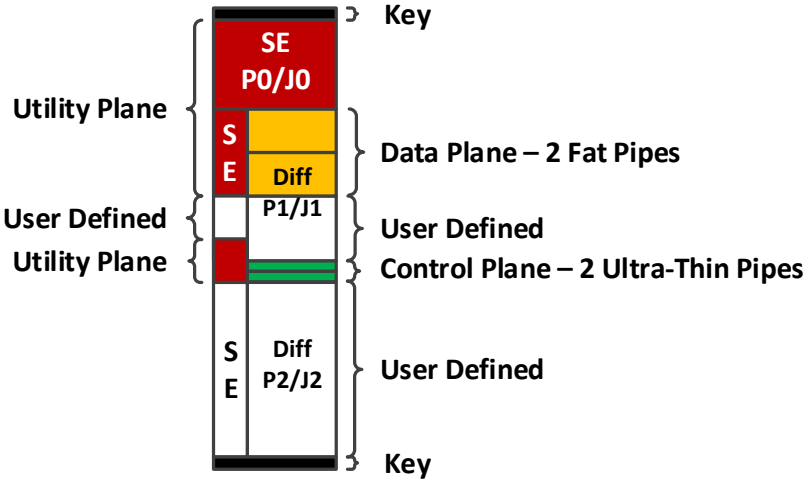

Figure 5-3 – HOST Payload Slot Profile, SLT3-PAY-2F2U-HOST

T2-RUL-0145: If 3U Payload Modules implement the Data Plane, Payload Modules **shall** implement the first Data Plane fat pipe as defined by ANSI/VITA 65.0, section 14.2.3.3.

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T2-PER-0048: 3U Payload Modules **may** implement both Data Plane fat pipes as defined by ANSI/VITA 65.0, section 14.2.3.3.

T2-OBS-0155: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.3.1.2.

T2-RUL-0146: If 3U Payload Modules implement the Control Plane, Payload Modules **shall** implement the first Control Plane ultra-thin pipe as defined by ANSI/VITA 65.0, section 14.2.3.2.

T2-PER-0049: 3U Payload Modules **may** implement both Control Plane ultra-thin pipes as defined by ANSI/VITA 65.0, section 14.2.3.2.

T2-OBS-0156: The OpenVPX Control Plane is part of both the SCTI and CMTI as defined in SECTION 5.3.1.2 and SECTION 5.3.1.5.

T2-OBS-0157: Reserved signals cannot be utilized for any other purpose (such as user I/O).

5.1.1.1.3.2 3U Module Profiles, MOD3-PAY-2F2U-HOST

Table 5-2 – HOST Module Profiles, MOD3-PAY-2F2U-HOST

Profile Name	Data Plane 2 FP		Control Plane 2 UTPs	
	DP01	DP02	CPutp01	CPutp02
MOD3-PAY-2F2U-HOST1	10GBase-KX4 Ethernet per ANSI/VITA 65.0 section 5.1.5	10GBase-KX4 Ethernet per ANSI/VITA 65.0 section 5.1.5	1000BASE-KX or BX per ANSI/VITA 46.6	
MOD3-PAY-2F2U-HOST2	PCIe per ANSI/VITA 65.0 section 5.3	PCIe per ANSI/VITA 65.0 section 5.3	1000BASE-KX or BX per ANSI/VITA 46.6	
MOD3-PAY-2F2U-HOST3	10GBase-KX4 Ethernet per ANSI/VITA 65.0 section 5.1.5	PCIe per ANSI/VITA 65.0 section 5.3	1000BASE-KX or BX per ANSI/VITA 46.6	

T2-OBS-0158: The following ANSI/VITA 65.0 Module Profiles are compatible with MOD3-PAY-2F2U-HOST:

- MOD3-PAY-2F2U-16.2.3-2
- MOD3-PAY-2F2U-16.2.3-3
- MOD3-PAY-2F2U-16.2.3-5

T2-PER-0050: 3U Payload Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR Ethernet per clause 72 of IEEE 802.3. Note that it will still need to be able to support 10GBase-KX4.

T2-PER-0051: 3U Payload Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0147: 3U Payload Modules using 10GBASE-KR **shall** comply with clause 72 of IEEE 802.3.

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T2-OBS-0159: If implementing 10GBASE-KR the pin mapping should still comply with ANSI/VITA 46.6 but ANSI/VITA 46.7, section 5 should be consulted for electrical requirements and channel compliance.

T2-OBS-0161: A specific version of PCIe is not called out in this profile to allow for future generations of PCIe.

5.1.1.1.3.3 3U Payload Module with Mezzanine Site Requirements

T2-RUL-0148: 3U Payload Module mezzanine sites configured to exclusively support a PMC Mezzanine **shall** conform to ANSI/VITA 46.9, section 4.1 regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0149: 3U Payload Module mezzanine sites configured to exclusively support a XMC Mezzanine **shall** conform to one of the following options regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector:

1. ANSI/VITA 46.9, section 4.4, X24s+X8d+X12d.
2. Only the P1w9-x12d portion of ANSI/VITA 46.9, section 4.6.

T2-RUL-0151: 3U Payload Module mezzanine sites configured to support both PMC and XMC Mezzanines **shall** conform to ANSI/VITA 46.9, section 4.2 regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

5.1.1.1.3.4 3U HOST Payload Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements

T2-PER-0054: 3U Payload Modules **may** replace the P2 connector with an ANSI/VITA 66.0 or ANSI/VITA 67.0 compliant blind mate connector.

T2-RUL-0152: If following Permission 0046, 3U Payload Modules **shall** only replace the P2 connector.

T2-RUL-0153: 3U Payload Modules **shall** exclusively use blind mate Fiber Optic interconnects defined in ANSI/VITA 66.0 and its related dot standards for interfacing with fiber optic cables.

T2-RUL-0154: 3U Payload Modules using optical interconnects **shall** conform to the requirements of the chosen blind mate connector's respective ANSI/VITA 66.0 dot standard.

T2-PER-0052: If using the ANSI/VITA 66.0 half width variant, a 3U Payload Module **may** utilize an RT-2 or RT-2R Backplane Full Right and Backplane center connector per ANSI/VITA 66.0 to fill out the rest of the 2F2U-HOST Slot Profile connections.

T2-RUL-0155: 3U Payload Modules using coaxial interconnects **shall** exclusively use the blind mate Coaxial interconnect defined in ANSI/VITA 67.1.

T2-RUL-0156: 3U Payload Modules using coaxial interconnects **shall** conform to the requirements of ANSI/VITA 67.1.

T2-PER-0053: If using the ANSI/VITA 67.1 coaxial interconnect, a 3U Payload Module **may** utilize an RT-2 or RT-2R Backplane Full Right and Backplane center connector per ANSI/VITA 67.1 to fill out the rest of the 2F2U-HOST Slot Profile connections.

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5.1.1.2 Power Supply Modules

5.1.1.2.1 Common 6U and 3U Power Supply Module Requirements

T2-RUL-0310: PSM requirements **shall** be applied using the following order of precedence:

1. Requirements of this Tier 2 HOST Standard (including additions or exclusions to ANSI/VITA 65.0)
2. Requirements of ANSI/VITA 62.0

T2-OBS-0170: PSMs can be configured as a single-stage or two-stage power supply system as specified by ANSI/VITA 62.0, section 1.2.

T2-OBS-0180: PSMs can utilize energy storage modules as specified by ANSI/VITA 62.0 to satisfy target-system power hold-up requirements.

T2-PER-0060: PSMs **may** monitor the power rails and generate a SYRESET* per ANSI/VITA 62.0, Permission 3.1-1.

T2-RUL-0320: PSMs **shall** assert the FAIL* signal when PO1, PO2, PO3, or AUX voltages are not within their voltage specifications per ANSI/VITA 62.0, Recommendation 3.3-2.

T2-RUL-0330: PSMs that accept external prime input power **shall** do so in accordance with ANSI/VITA 62.0, section 6.5.1.

T2-OBS-0190: PSMs that accept external prime input power include Single-Stage Power Subsystem Modules and Front-End Modules of Two-Stage Power Subsystems.

T2-RUL-0340: PSMs that supply power to the payload/switch slot portion of the Backplane **shall** output +12V final power in accordance with ANSI/VITA 62.0, section 4.6.1.2.

T2-RUL-0350: PSMs that supply power to the payload/switch slot portion of the Backplane **shall** output +5V final power in accordance with ANSI/VITA 62.0, section 4.6.1.5.

T2-RUL-0360: PSMs that supply power to the payload/switch slot portion of the Backplane **shall** output 3.3V_AUX in accordance with ANSI/VITA 62.0, section 4.6.1.7.

T2-RUL-0370: PSMs that supply power to the payload/switch slot portion of the Backplane **shall** output +/-12V AUX in accordance with ANSI/VITA 62.0, section 4.6.1.8.

T2-OBS-0200: PSMs supplying power to payloads/switches include Single-Stage Power Subsystem Modules and Back-End Modules of a Two-Stage Power Subsystem.

T2-OBS-0210: The ANSI/VITA 62.0 requirements for +48V final power are not applicable to this Tier 2 Core Technology Standard.

T2-RUL-0371: PSMs **shall** have the CHASSIS pin connected to their front panel and covers.

T2-RUL-0372: PSMs **shall** have the CHASSIS pin isolated from the SIGNAL_RETURN pin.

T2-RUL-0373: PSMs **shall** have the CHASSIS pin isolated from power returns, such as the POWER_RETURN pins.

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T2-RUL-0374: PSMs **shall** have the CHASSIS pin isolated from the -DC_IN/ACN pin.

T2-OBS-0205: The rules for isolating the CHASSIS pins come from ANSI/VITA 62.0, Recommendations in section 4.7.

T2-RUL-0380: PSMs outputting an intermediate power **shall** explicitly define the nominal voltage level for the intermediate power.

T2-RUL-0390: PSMs having intermediate power as an input **shall** explicitly define the nominal voltage level for the intermediate power.

T2-OBS-0220: The SPDI is implemented using the OpenVPX Utility Plane as well as additional requirements specified herein.

T2-OBS-0230: PSMs make use of a subsection of the CMTI OpenVPX Utility Plane since they do not contain traditional processing elements.

5.1.1.2.1.1 Common Energy Storage Module Requirements

T2-RUL-0480: Energy Storage Modules **shall** accept an input of the intermediate voltage in accordance with ANSI/VITA 62.0, section 4.5.

T2-RUL-0490: Energy Storage Modules **shall** output the intermediate voltage in accordance with ANSI/VITA 62.0, section 4.5.

5.1.1.2.2 6U Power Supply Module Requirements

T2-RUL-0270: 6U PSMs **shall** conform to the requirements of ANSI/VITA 62.0 for 6U Modular Power Supplies except where specified herein.

T2-RUL-0300: 6U PSMs **shall** conform to the mechanical requirements of ANSI/VITA 65.0 for 6U conduction cooled modules except where specified herein.

5.1.1.2.2.1 6U Front-End Module Requirements

T2-RUL-0460: 6U Front-End Modules **shall** route the intermediate voltage to pins in accordance with ANSI/VITA 62.0, section 4.6.2.1.2.

5.1.1.2.2.2 6U Back-End Module Requirements

T2-RUL-0470: 6U Back-End Modules **shall** accept an input of the intermediate voltage in accordance with ANSI/VITA 62.0, section 6.5.1.

5.1.1.2.2.3 6U Single-Stage Module Requirements

T2-RUL-0500: 6U Single-Stage Modules **shall** route the intermediate voltage to the ANSI/VITA 62.0 pins labeled “POS_FILT_OUT” and “NEG_FLT_OUT” in accordance with ANSI/VITA 62.0, section 6.5.2.

5.1.1.2.3 3U Power Supply Module Requirements

T2-RUL-0501: 3U PSMs **shall** conform to the requirements of ANSI/VITA 62.0 for 3U Modular Power Supplies except where specified herein.

T2-RUL-0502: 3U PSMs **shall** conform to the mechanical requirements of ANSI/VITA 65.0 for 3U conduction cooled modules except where specified herein.

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T2-RUL-0503: 3U PSMs that supply power to the payload/switch slot portion of the Backplane **shall** output +3.3V final power in accordance with ANSI/VITA 62.0, section 4.6.1.4.

5.1.1.2.3.1.1 **3U Front-End Module Requirements**

T2-RUL-0504: 3U Front-End Modules **shall** route the intermediate voltage to pins in accordance with ANSI/VITA 62.0, section 4.6.2.1.1.

5.1.1.2.3.1.2 **3U Back-End Module Requirements**

T2-RUL-0505: 3U Back-End Modules **shall** accept an input of the intermediate voltage in accordance with ANSI/VITA 62.0, section 5.5.1.

5.1.1.3 **Switch Modules**

When using multiple Payload Modules it is often necessary to utilize a Switch Module to accomplish the necessary communication. This HOST Standard utilizes two unmodified ANSI/VITA 65.0 switch slot and Module Profiles.

5.1.1.3.1 **Common 6U and 3U HOST Switch Requirements**

T2-RUL-0531: Switch Modules **shall** implement the requirements of ANSI/VITA 65.0, section 3.7 (OpenVPX ANSI/VITA 46.0 Connector P0/J0 and P1/J1 Connector Pin Assignments).

T2-RUL-0534: Switch Modules **shall** be designed to accommodate any combination of power supply power up and power down sequences without causing board failure.

T2-RUL-0535: Switch Modules **shall** follow the rules of ANSI/VITA 46.0, section 4.8.3 System Controller.

T2-PER-0061: Switch Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0511: Switch Modules using 10GBASE-KR **shall** comply with clause 72 of IEEE 802.3.

T2-OBS-0235: If implementing 10GBASE-KR the pin mapping should still comply with ANSI/VITA 46.6 but ANSI/VITA 46.7, section 5 should be consulted for electrical requirements and channel compliance.

T2-PER-0062: Switch Modules **may** combine Control Plane ultra-thin pipes to create Control Plane fat pipes.

T2-OBS-0237: It may be necessary to combine 4 10GBASE-KR ultra-thin pipes to create a single 40GBase-KR fat pipe.

T2-RUL-0536: Switch Modules **shall** implement the Utility Plane requirements as defined in SECTION 5.3.1.5.1.1.

5.1.1.3.2 **6U Switch Module Requirements**

T2-RUL-0520: 6U Switch Modules **shall** be implemented as 6U OpenVPX Switch Plug-In Modules per SECTION 5.3.2.2.

T2-RUL-0530: 6U Switch Modules **shall** conform to the 6U conduction cooled requirements of ANSI/VITA 65.0, section 12.1.1.

T2-RUL-0533: 6U Switch Modules **shall** follow ANSI/VITA 65.0, section 12.1.2 with regards to Power Voltages and System Management.

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T2-RUL-0532: 6U Switch Modules **shall** conform to 6U Switch Profile 1 or 6U Switch Profile 2.

5.1.1.3.2.1 **6U Switch Profile 1: SWH-20U19F**

T2-RUL-0540: 6U Switch Profile 1 Modules **shall** conform to the Slot Profile SLT6-SWH-20U19F-10.4.1 per ANSI/VITA 65.0, section 10.4.1 except for section 10.4.1.1 Utility Plane.

T2-RUL-0550: 6U Switch Profile 1 Modules **shall** conform to one of the Module Profiles in TABLE 5-3.

Table 5-3 – HOST 20U19F Switch Module Profiles, MOD6-SWH-20U19F-HOST

Profile Name	Control Plane 20 UTP		Data Plane 19 UTP	
	Inter-Switch or Payload Slots CSutp01 to CSutp04	**Payload Slots CPutp01 to CPutp16**	**Payload Slots DP01 to DP15**	**Inter –Switch or Payload Slots DS01 to DS04**
MOD6-SWH-20U19F-HOST1	1000BASE-KX or BX per ANSI/VITA 46.6		10GBase-KX4 Ethernet per ANSI/VITA 65.0 section 5.1.5	
MOD6-SWH-20U19F-HOST2	1000BASE-KX or BX per ANSI/VITA 46.6		PCIe per ANSI/VITA 65.0 section 5.3	

T2-OBS-0238: Note that the MOD6-SWH-20U19F-HOST2 switch has PCIe in the Data Plane, but this is the profile that would be used in a system that wants to utilize HOST Payload's PCIe Expansion Plane as a switched network. Due to the Expansion Plane being primarily used for adjunct modules, the OpenVPX ecosystem does not contain Expansion Plane Switch Modules.

5.1.1.3.2.2 **6U Switch Profile 2: SWH-16U20F**

T2-RUL-0560: 6U Switch Profile 2 Modules **shall** conform to the Slot Profile SLT6-SWH-16U20F-10.4.2 per ANSI/VITA 65.0, section 10.4.2 except for section 10.4.2.1 Utility Plane.

T2-RUL-0570: 6U Switch Profile 2 Modules **shall** conform to one of the Module Profiles in TABLE 5-4.

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Table 5-4 – HOST 16U20F Switch Module Profiles, MOD6-SWH-16U20F-HOST

Profile Name	Control Plane 16 UTP		Data Plane 20 UTP	
	Inter-Switch or Payload Slots CSutp01 to CSutp04	**Payload Slots CPutp01 to CPutp12**	**Payload Slots DP01 to DP16**	**Inter –Switch or Payload Slots DS01 to DS04**
MOD6-SWH-16U20F-HOST1	1000BASE-KX or BX per ANSI/VITA 46.6		10GBase-KX4 Ethernet per ANSI/VITA 65.0 section 5.1.5	
MOD6-SWH-16U20F-HOST2	1000BASE-KX or BX per ANSI/VITA 46.6		PCIe per ANSI/VITA 65.0 section 5.3	

T2-OBS-0239: Note that the MOD6-SWH-16U20F-HOST2 switch has PCIe in the Data Plane. This is the profile that would be used in a system that wants to utilize HOST Payload's PCIe Expansion Plane as a switched network. Due to the Expansion Plane being primarily used for adjunct modules, the OpenVPX ecosystem does not contain Expansion Plane Switch Modules.

5.1.1.3.2.3 6U Switch Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements

T2-PER-0064: 6U Switch Modules **may** replace the P6 connector with an ANSI/VITA 66.0 or ANSI/VITA 67.0 compliant blind mate connector.

T2-RUL-0561: If following Permission 0064, 6U Switch Modules **shall** only replace the P6 connector.

T2-PER-0065: 6U Switch Modules **may** replace the P5 and P6 connector with an ANSI/VITA 66.0 or ANSI/VITA 67.0 compliant blind mate connector.

T2-RUL-0562: If following Permission 0065, 6U Switch Modules **shall** only replace the P5 and P6 connectors.

T2-RUL-0563: 6U Switch Modules using fiber optic interconnects **shall** exclusively use blind mate Fiber Optic interconnects defined in ANSI/VITA 66.0 and its related dot standards for interfacing with fiber optic cables.

T2-RUL-0564: 6U Switch Modules using optical interconnects **shall** conform to the requirements of the chosen blind mate connector's respective ANSI/VITA 66.0 dot standard.

T2-RUL-0565: 6U Switch Modules using fiber optic interconnects **shall** use full width variants of the Fiber Optic blind mate connectors.

T2-RUL-0566: 6U Switch Modules using optical interconnects **shall** exclusively use the blind mate Coaxial interconnect defined in ANSI/VITA 67.2.

T2-RUL-0567: 6U Switch Modules using coaxial interconnects **shall** conform to the requirements of ANSI/VITA 67.2.

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5.1.1.3.3 **3U Switch Module Requirements**

T2-RUL-0568: 3U Switch Modules **shall** be implemented as 3U OpenVPX Switch Plug-In Modules per SECTION 5.3.2.2.

T2-RUL-0569: 3U Switch Modules **shall** conform to the 3U conduction cooled requirements of ANSI/VITA 65.0, section 16.1.1.

T2-RUL-0571: 3U Switch Modules **shall** follow ANSI/VITA 65.0, section 16.1.2 with regards to Power Voltages and System Management.

T2-RUL-0572: 3U Switch Modules **shall** conform to 3U Switch Profile 1 or 3U Switch Profile 2.

5.1.1.3.3.1 **3U Switch Profile 1: SWH-6F6U**

T2-RUL-0573: 3U Switch Profile 1 Modules **shall** conform to the Slot Profile SLT3-SWH-6F6U-14.4.1 per ANSI/VITA 65.0, section 14.4.1 except for section 14.4.1.1.

T2-RUL-0574: 3U Switch Profile 1 Modules **shall** implement the external connection thin pipe per ANSI/VITA 65.0, section 14.4.1.4.1.

T2-RUL-0575: 3U Switch Profile 1 Modules **shall** conform to Module Profile MOD3-SWH-6F6U-16.4.1-3 or MOD3-SWH-6F6U-16.4.1-5 per ANSI/VITA 65.0, section 16.4.1.

T2-PER-0066: 3U Switch Profile 1 modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR Ethernet per clause 72 of IEEE 802.3. Note that it will still need to be able to support 10GBase-KX4.

T2-PER-0067: 3U Switch Profile 1 Modules **may** utilize a different generation of PCIe than what is called out in the Module Profile.

5.1.1.3.3.2 **3U Switch Profile 2: SWH-32U**

T2-RUL-0576: 3U Switch Profile 2 Modules **shall** conform to the Slot Profile SLT3-SWH-32U-HOST per FIGURE 5-4.

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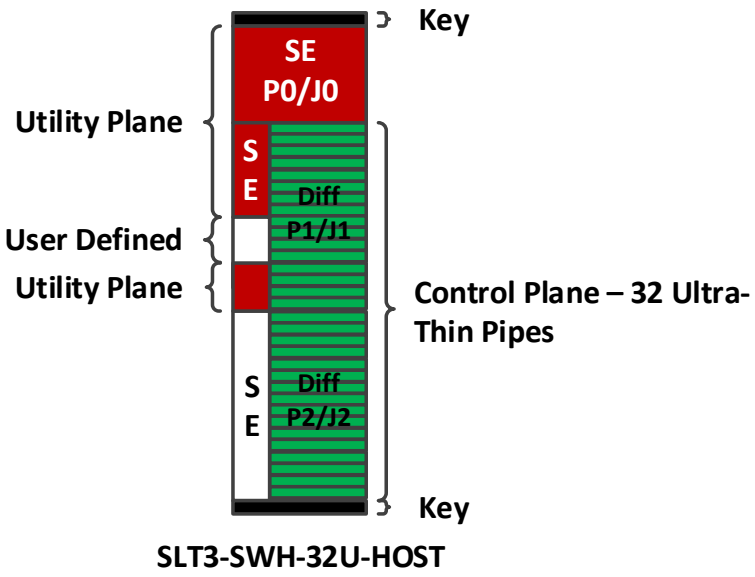

Figure 5-4– Switch Profile, SLT3-SWH-32U-HOST

T2-RUL-0577: 3U Switch Profile 2 Modules **shall** implement the Utility Plane requirements as defined in SECTION 5.3.1.5.1.1.

T2-RUL-0578: 3U Switch Profile 2 Modules **shall** implement the Control Plane ultra-thin pipes per ANSI/VTA 65.0, section 6.2.2.

T2-RUL-0579: 3U Switch Profile 2 Modules **shall** designate unused ultra-thin pipe signals as Reserved.

T2-OBS-0241: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0581: 3U Switch Profile 2 Modules **shall** conform to the Module Profile MOD3-SWH-32U-HOST per TABLE 5-5.

Table 5-5 – HOST Module Profile, MOD3-SWH-32U-HOST

Profile Name	Control Plane 32 UTPs	
	CPutp01	CPutp02
MOD3-SWH-32U-HOST	1000BASE-KX or BX per ANSI/VITA 46.6	

5.1.1.3.3.3 3U Switch Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements

T2-PER-0068: 3U Switch Modules **may** replace the P2 connector with an ANSI/VITA 66.0 or ANSI/VITA 67.0 compliant blind mate connector.

T2-RUL-0582: If following Permission 0064, 3U Switch Modules **shall** only replace the P2 connector.

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T2-RUL-0583: 3U Switch Modules using Backplane Fiber Optic interconnects **shall** use blind mate Fiber Optic interconnects defined in ANSI/VITA 66.0 and its related dot standards for interfacing with fiber optic cables.

T2-RUL-0584: 3U Switch Modules using optical interconnects **shall** conform to the requirements of the chosen blind mate connector's respective ANSI/VITA 66.0 dot standard.

T2-PER-0069: If using the ANSI/VITA 66.0 half width variant, a 3U Switch Module **may** utilize an RT-2 or RT-2R Backplane Full Right and Backplane center connector per ANSI/VITA 66.0 to fill out the rest of the chosen Switch Profile connections.

T2-RUL-0585: 3U Switch Modules using Backplane coaxial interconnects **shall** use the blind mate Coaxial interconnect defined in ANSI/VITA 67.1.

T2-RUL-0586: 3U Switch Modules using coaxial interconnects **shall** conform to the requirements of ANSI/VITA 67.1.

T2-PER-0071: If using the ANSI/VITA 67.1 coaxial interconnect, a 3U Switch Module **may** utilize an RT-2 or RT-2R Backplane Full Right and Backplane center connector per ANSI/VITA 67.1 to fill out the rest of the chosen Switch Slot Profile connections.

5.1.2 Mezzanine Requirements

5.1.2.1 Common Mezzanine Requirements

HOST Mezzanine Modules are HOST Modules that mount onto a HOST Payload Module. The two types of HOST Mezzanine form factors are PMC and XMC.

T2-RUL-0590: Requirements for Mezzanines **shall** be applied using the following order of precedence:

1. Requirements of this HOST Tier 2 Standard (including additions or exclusions to PMC/XMC standards)
2. Mezzanine Module requirements of IEEE 1386.1 and ANSI/VITA 42.0 for PMCs and XMCs respectively

T2-RUL-0600: Mezzanines **shall** perform all of their required I/O functions through their mezzanine connectors.

T2-OBS-0240: Some sections of the mezzanine card standards contain requirements for mezzanine card front panel I/O. These requirements are not applicable to this Tier 2 technology. This Tier 2 technology only utilizes mezzanine card I/O that pass through the mezzanine card connector.

T2-RUL-0610: Mezzanines **shall** conform to the interface requirements of the SCTI for Mezzanine Modules per SECTION 5.3.1.2.

T2-OBS-0250: The SCTI for PMCs is implemented using OpenVPX high-speed serial interconnects to PCI bridging as defined in SECTION 1.1.1.1.1.

T2-OBS-0260: The CMTI for Mezzanines is implemented using the OpenVPX Utility Plane in conjunction with the appropriate mezzanine card standard defined in SECTION 5.3.1.5.

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T2-OBS-0270: The SPDI for Mezzanines is implemented using the OpenVPX Utility Plane in conjunction with the appropriate mezzanine card standard defined in SECTION 5.3.1.6.

T2-PER-0070: A Mezzanine connector that has no signals routed to it **may** be left unpopulated.

T2-PER-0080: A Mezzanine connector **may** leave a user defined signal as a no connect if the signal is not implemented in the mezzanine design.

5.1.2.2 XMC Mezzanine Requirements

T2-RUL-0620: XMC Mezzanines **shall** conform to the requirements of ANSI/VITA 42.0 Standard for Switched Mezzanine Cards (herein referred to as XMC).

T2-RUL-0640: XMC Mezzanines **shall** conform to ANSI/VITA 46.9, section 3.3, section 3.5, and section 3.6 regarding XMC connector I/O mapping.

T2-RUL-0650: XMC Mezzanines that do not require utilization of all available user I/O signals **shall** leave the remaining unused signals as no connects.

5.1.2.3 PMC Mezzanine Requirements

T2-RUL-0660: PMC Mezzanines **shall** conform to the requirements of IEEE Std. 1386.1 Standard for PCI Mezzanine Cards (referred to as PMC).

T2-RUL-0680: PMC Mezzanines **shall** conform to ANSI/VITA 46.9, section 3.2 regarding PMC connector I/O mapping.

T2-RUL-0690: PMC Mezzanines that do not require utilization of all available user I/O signals **shall** leave the remaining unused signals as no connects.

T2-RUL-0700: If a PMC Mezzanine is implementing a 64-bit PCI bus for PMC communication, a PMC Mezzanine **shall** populate a minimum of Pn1, Pn2, Pn3, and Pn4.

T2-RUL-0710: If a PMC Mezzanine is implementing a 32-bit PCI bus for PMC communication, a PMC Mezzanine **shall** populate a minimum of Pn1, Pn2, and Pn4.

5.2 HOST Management

HOST Management (HOST-MGMT) establishes an autonomous subsystem that provides application independent hardware management and monitoring capabilities for the module, chassis, and system domains. The inclusion of HOST-MGMT in the HOST Standard is intended to ensure completeness in the specification of all hardware, software, and firmware necessary to implement and standardize the management functions and interfaces. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

5.2.1 Logical Control Elements

HOST-MGMT implements logical control elements known as the Manager, Participants, and Remote Participants that are used in the context of a communication protocol to coordinate messaging between HOST Modules and to perform general chassis management duties. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

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The HOST Tier 2 OpenVPX Core Technology is based on the ANSI/VITA 46.11 standard System Management on VPX, which in turn leverages both the IPMI standard and the PICMG Advanced TCA (ATCA) 3.0 standard. This Tier 2 HOST standard defines an architecture that supports the implementation of these logical control elements to form an intelligent management subsystem within the context of a VPX system comprised of HOST Modules. The foundation provided by the core technology is augmented with HOST-specific management requirements for completeness.

HOST-MGMT utilizes Participants to perform low-level hardware management and to communicate on the CMTI. Participant implementation strategies can vary, e.g. Payload processor software implementation, COTS chipsets, FPGAs, SoCs, etc.

HOST-MGMT functionality may not be fully contained within COTS solutions and can be supplemented by additional HOST-MGMT components. HOST-MGMT accesses the CMTI via the Participant. HOST-MGMT for this Core Technology Standard can leverage ANSI/VITA 46.11 and IPMI with additional functional requirements defined in this document.

The CMTI, defined in Tier 1, is further specified by this Tier 2 HOST Standard. The CMTI is primarily a logical interface. The HOST Manager for this Tier 2 Core Technology Standard is a derivative of the ANSI/VITA 46.11 chassis manager that is augmented with HOST-specific management requirements. A HOST Manager may access the IPMB or Control Plane through a dedicated Controller, a link that is native to the hosting CPU, or through the Participant for the hosting Module if the Participant provides Manager "pass-through" communication capabilities.

5.2.1.1 **Manager**

The Manager is an entity that manages Participants within the Chassis Domain. The Manager communicates with Participants via the HOST CMTI utilizing the HOST MPP. There is exactly one entity acting as a Manager in the *HOST Chassis* at any given time. There may be one or more *Standby Managers* capable of taking over Manager duties. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

The Manager for this Core Technology Standard leverages the functionality of the chassis manager, as defined in ANSI/VITA 46.11 and IPMI, implemented within the GPR. As a Chassis Domain entity, the Manager is not required to be physically located on a specific HOST Module or piece of hardware within the chassis, but can reside anywhere as specified by the target-system requirements.

T2-RUL-0720: The Manager **shall** perform chassis management utilizing the system management bus pins SM[1..0] (IPMB-A) as defined by ANSI/VITA 65.0, section 3.4.5, System Management Buses, and/or the Control Plane.

T2-REC-0015: The Manager **should** perform chassis management utilizing the system management bus pins SM[3..2] (IPMB-B) as defined by ANSI/VITA 65.0, section 3.4.5, System Management Buses.

T2-OBS-0280: The system management buses SM[3..0] represent the physical lines used for management communications. These data lines also make up a portion of the CMTI. See SECTION 5.3.1.5 for more details about the CMTI.

T2-RUL-0728: If the Manager implements chassis management over the Control Plane, then the Manager **shall** perform the communication in compliance with IPMI, SECTION 13 "IPMI LAN Interface."

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T2-RUL-0730: Managers **shall** conform to the requirements of ANSI/VITA 46.11 section 5.1.1 “Basic Chassis Manager IPMI Requirements.”

T2-RUL-0731: The Manager **shall** have the ability to detect the assertion of its Plug-In slot’s SYS_CON* signal.

T2-REC-0016: Upon Startup, the Manager **should** be determined by an assertion of a Plug-In slot’s SYS_CON* signal.

T2-RUL-1940: A Manager **shall** send a Set Event Receiver Message with the Event Receiver Slave Address field set 0x20.

T2-OBS-0440: The Manager is responsible for ensuring that all Participants in the chassis have successfully received and processed the Set Event Receiver Message.

T2-OBS-0450: Setting the Event Receiver Slave Address to the Manager’s address of 0x20 designates this address as the Event Receiver. See IPMI section 29.1 for information on the Set Event Receiver Message.

T2-OBS-0470: Having the Manager send a Set Event Receiver Message mandates that all Intelligent Platform Management Controllers (IPMCs) on the IPMB be ANSI/VITA 46.11 Tier-2 Capable (ANSI/VITA 46.11 section 4).

T2-RUL-2121: Managers **shall** maintain a Chassis SDR Repository in accordance with ANSI/VITA 46.11 section 6.3.

T2-RUL-2122: Managers **shall** maintain a Chassis System Event Log in accordance with ANSI/VITA 46.11 section 7.

T2-OBS-0475: Managers will correspond to the ANSI/VITA 46.11 requirements for a Tier-2 Chassis Manager.

5.2.1.2 **Participant**

A Participant is a software or firmware entity that resides on a HOST Module and manages the Module Domain functional resources on that HOST Module. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

T2-RUL-0755: Participants **shall** utilize the system management buses SM[1..0] (IPMB-A) as defined by ANSI/VITA 65.0, section 3.4.5, System Management Busses, and/or the Control Plane for MPP communication.

T2-REC-0025: Participants **should** perform chassis management utilizing the system management buses SM[3..2] (IPMB-B) as defined by ANSI/VITA 65.0, section 3.4.5, System Management Busses.

T2-RUL-0756: If a Participant utilizes the Control Plane for MPP communication, then the Participant **shall** perform the communication in compliance with IPMI, section 13 “IPMI LAN Interface.”

T2-RUL-0760: Participants **shall** adhere to the SYSRESET* requirements of ANSI/VITA 46.11 section 4.1.9, IPMC Resets.

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T2-OBS-0290: The SYSRESET* requirements of ANSI/VITA 46.11 section 4.1.9, IPMC Resets, supersede the requirements of ANSI/VITA 65.0.

T2-RUL-0770: Participants **shall** conform to the requirements of ANSI/VITA 46.11 section 4.1.1 "IPMI Communication."

T2-OBS-0772: Participants are analogous with the requirements of a 46.11 IPMC, the greatest difference being the capability of communicating over the Control Plane.

T2-OBS-0300: A Participant may not be able to process a *Command* from a Manager if a fault has occurred on the HOST Module that is preventing a Participant from processing and executing the Command. The Participant could also be processing a previous Command and not have the ability to immediately respond to the Manager's Command.

T2-PER-0085: Participants **may** be exempted from transmitting MPP Messages based on Platform security requirements.

T2-OBS-0295: Platform security requirements will be defined in the Tier 3 Component Specifications.

T2-RUL-1945: Participants that are enabled for event generation **shall** send active event messages to the location indicated in the "Set Event Receiver" message when events are detected.

T2-OBS-0501: Per ANSI/VITA 46.11, the Set Event Receiver Message enables Participants to send Sensor Event messages upon the detection of a change in sensor status. These messages can therefore be sent based on the Participant's determination of need, and not always in direct response to a Command from the Manager.

T2-RUL-1946: All Participants **shall** adhere to the Tier-2 IPMC rules of ANSI/VITA 46.11 section 7.

T2-RUL-1947: All Participants **shall** adhere to ANSI/VITA 46.11 section 6.1.

T2-RUL-1948: All Participants **shall** adhere to ANSI/VITA 46.11 section 6.2.

5.2.1.3 **Remote Participant**

A Remote Participant is a software or firmware entity that resides on a HOST Module and represents a *Proxied HOST Module* that is not capable of communicating in a manner consistent with MPP. A Proxied HOST Module is represented by a Remote Participant that incorporates a Proxy implementing software, firmware, and/or hardware translation. Because the Participant that represents the HOST Module to the Manager is fully conformant to MPP, the Proxy is transparent to the Manager. A Remote Participant consequently has no additional requirements at the Tier 2 level. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

5.2.1.4 **IPMI Security**

IPMI has known security concerns and presents the potential for an attacker to compromise confidentiality, integrity, and availability if vulnerabilities are not understood and addressed. It is critical to protect against threats to the physical-level access to the hardware that could be used to reboot the system, install malware, compromise data, or bypass operating system controls. Most IPMI related risks can be mitigated through configuration settings and process safeguards that place appropriate limits on its use within the context of military applications, but it is ultimately the

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responsibility of the Platform integrator and safety certification authorities to determine if these mitigations are sufficient for any particular system. United States Computer Emergency Readiness Team (US-CERT) Alert (TA13-207A) “Risks of Using the Intelligent Platform Management Interface (IPMI)” provides additional details and recommendations regarding IPMI security.

T2-RUL-1949: HOST Modules supporting IPMI **shall** be, at minimum, configurable in a way that is consistent with US-CERT Alert TA13-207A security recommendations.

T2-REC-0017: System requirements **should** carefully consider the implications of transmitting classified data on the IPMI bus or handling classified data within access of the related hardware components and include appropriate architectural and design decisions to ensure security requirements are satisfied.

5.2.2 System Management Architecture

The system management architecture is hierarchical in nature with the system manager at the highest level. The system manager will communicate with the chassis manager at the next level. The chassis manager will then communicate with the Participants at the lowest level.

This standard does not require or restrict the presence of multiple manager entities in a chassis. However, if there are redundant Managers implemented in a chassis only one Manager can be active at any one time. Failover logic and implementation details are not given in this standard. It is up to the system integrator to ensure proper failover logic and communication between Managers.

The system management topology is not addressed in this standard. There are no restrictions on having a bussed topology versus a radial or star topology. However, the unrestricted nature of the Manager as it is defined in this standard inhibits the ability to use a radial or star topology if more than one Manager is implemented in the chassis. Attention to this detail must be taken into consideration by the system integrator when defining the system management architecture.

5.2.3 Inventory Information Records and Event Logs

Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

5.2.3.1 Inventory Information Records

Inventory Information Records will be maintained to provide a means of preserving and verifying manufacturer hardware product information. Participants maintain *Module Domain Inventory Information Records* that contain the hardware specific information necessary to verify its HOST Module. The Manager maintains a *Chassis Domain Inventory Information Record* that contains additional chassis-specific information and can be used to verify the chassis configuration against the Module Domain Inventory Information Records. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

T2-RUL-0810: Participants **shall** conform to the requirements as specified in ANSI/VITA 46.11 section 8.1 "Board FRU Information."

T2-OBS-0305: The Board FRU Information section in ANSI/VITA 46.11 defines requirements that will be utilized for the Module Domain Inventory Information Record.

T2-RUL-0820: The Manager **shall** conform to the requirements as specified in ANSI/VITA 46.11 section 8.2 “Chassis FRU Information.”

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T2-OBS-0306: The Chassis FRU Information section in ANSI/VITA 46.11 defines requirements that will be utilized for the Chassis Domain Inventory Information Record.

5.2.3.2 Event Logs

HOST-MGMT Event Logs are maintained for the storage of hardware events, faults, and anomalies. Participants maintain *Module Domain Event Logs* that contain a record of events for the HOST Module the Participant is representing. The Manager collects aggregate event status that represents all Participant reported events. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

T2-RUL-0821: Participants **shall** implement, in either volatile or non-volatile memory, a System Event Log as defined in IPMI, section 31 "System Event Log (SEL) Commands" and section 32 "SEL Record Formats."

T2-RUL-0822: The Manager **shall** implement a System Event Log as defined in IPMI, section 31 "System Event Log (SEL) Commands" and section 32 "SEL Record Formats."

T2-OBS-0307: The System Event Log will be utilized for the Module Domain Event Log and Chassis Domain Event Log.

5.2.4 Manager/Participant Protocol

HOST-MGMT defines communication between the Manager and Participants using a standardized means of data exchange known as MPP. Refer to the Tier 1 Standard for a complete description of associated activities and responsibilities.

The MPP is primarily derived from ANSI/VITA 46.11 which uses the message formatting defined in the IPMI Standard. The MPP messages are transmitted and received using the IPMB and/or the Control Plane, which are components of the CMTI. A subset of ANSI/VITA 46.11 messages (including those from IPMI) have been selected as mandatory messages that must be implemented for the MPP. All other messages defined in ANSI/VITA 46.11 and IPMI are optional for this HOST standard.

T2-RUL-0950: All MPP Messages **shall** be implemented using TABLE 5-6.

T2-PER-0951: IPMI and ANSI/VITA 46.11 messages in addition to those required **may** also be implemented.

T2-OBS-0340: ANSI/VITA 46.11 and IPMI V2.0 use the term "FRU" in some of the messages referenced in TABLE 5-6 below. Throughout this Tier 2 HOST Standard, "FRU" should be interpreted as "HOST Module."

Table 5-6 – ANSI/VITA 46.11 Messages

Message Name	Command	Network Function	Group ID	Standard Section
Get VSO Capabilities	00h	2Ch, 2Dh (Group Extension)	03h (VSO)	VITA 46.11, section 10.1.3.1
FRU Control	04h	2Ch, 2Dh (Group Extension)	03h (VSO)	VITA 46.11, section 10.1.3.6

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FRU Control Capabilities	1Eh	2Ch, 2Dh (Group Extension)	03h (VSO)	VITA 46.11, section 10.1.3.18
Set IPMB State	09h	2Ch, 2Dh (Group Extension)	03h (VSO)	VITA 46.11, section 10.1.3.7
Get FRU Address Info	40h	2Ch, 2Dh (Group Extension)	03h (VSO)	VITA 46.11, section 10.1.3.3
Get Mandatory Sensor Numbers	44h	2Ch, 2Dh (Group Extension)	03h (VSO)	VITA 46.11, section 10.1.3.26
Get Device ID	01h	06, 07 (App)	N/A	IPMI V2.0, section 20.1
Get Self-Test Results	04h	06, 07 (App)	N/A	IPMI V2.0, section 20.4
Get SEL Info	40h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.2
Get SEL Entry	43h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.5
Add SEL Entry	44h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.6
Partial Add SEL Entry	45h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.7
Clear SEL	47h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.9
Get SEL Time	48h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.10
Set SEL Time	49h	0A, 0B (Storage)	N/A	IPMI V2.0, section 31.11
Get FRU Inventory Area Info	10h	0A, 0B (Storage)	N/A	IPMI V2.0, section 34.1
Read FRU Data	11h	0A, 0B (Storage)	N/A	IPMI V2.0, section 34.2
Write FRU Data	12h	0A, 0B (Storage)	N/A	IPMI V2.0, section 34.3
Get Sensor Reading	2Dh	04, 05 (Sensor/Event)	N/A	IPMI V2.0, section 35.14
Get Device SDR Info	20h	04, 05 (Sensor/Event)	N/A	IPMI V2.0, section 35.2

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Get Device SDR	21h	04, 05 (Sensor/Event)	N/A	IPMI V2.0, section 35.3
Reserve Device SDR Repository	22h	04, 05 (Sensor/Event)	N/A	IPMI V2.0, section 35.4
Set Event Receiver	00h	04, 05 (Sensor/Event)	N/A	IPMI V2.0, section 29.1
Platform Event Message	02h	04, 05 (Sensor/Event)	N/A	IPMI V2.0, section 29.3

5.2.4.1 **Addressing**

HOST will use the addressing scheme defined in ANSI/VITA 46.11 for all MPP messages. The four uniquely defined addresses are:

1. VPX Hardware Address
2. IPMB Address
3. Physical Address
4. FRU Device ID

The Hardware Address for an OpenVPX Module is defined by seven bits, which are set by pin strappings in the OpenVPX connector. Each OpenVPX slot has a unique Hardware Address. The IPMB address is derived by multiplying the Hardware Address by 2. All devices communicating with the MPP use their IPMB address in the header of each IPMI message they send in order to identify themselves. The Physical Address is composed of a Site Type and Site Number. The Site Type is a high level description of the HOST Module (e.g. OpenVPX Module, XMC, Power Module, etc.). The Site Number designates a unique instance of the Site Type within the chassis. It is used to distinguish among HOST Module positions that have the same Site Type within the chassis. The FRU Device ID is used to identify Participants and Remote Participants. For example, a Participant in the form of an OpenVPX Plug-In Module, will have a Device ID of 0 and a PMC mezzanine installed on it and acting as a Remote Participant will have a Device ID of 1. Device IDs, along with the Physical Address, are used as data fields in IPMI messages to uniquely identify HOST Modules within a chassis.

T2-RUL-0960: The Manager **shall** conform to the VPX Hardware Address requirements of ANSI/VITA 46.11 section 4.1.4.1.2.

T2-RUL-0970: Participants **shall** conform to the VPX Hardware Address requirements of ANSI/VITA 46.11 section 4.1.4.1.2.

T2-RUL-0980: The Manager **shall** conform to the IPMB Address requirements of ANSI/VITA 46.11 section 4.1.4.2.

T2-RUL-0990: Participants **shall** conform to the IPMB Address requirements of ANSI/VITA 46.11 section 4.1.4.2.

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T2-RUL-1000: The Manager **shall** conform to the Physical Address requirements of ANSI/VITA 46.11 section 4.1.4.3.

T2-RUL-1010: Participants **shall** conform to the Physical Address requirements of ANSI/VITA 46.11 section 4.1.4.3.

T2-RUL-1020: The Manager **shall** conform to the FRU Device ID requirements of ANSI/VITA 46.11 section 4.1.4.5.

T2-RUL-1030: Participants **shall** conform to the FRU Device ID requirements of ANSI/VITA 46.11 section 4.1.4.5.

T2-RUL-1040: A Participant **shall** have an FRU Device ID of 0.

T2-OBS-0310: All ANSI/VITA 46.11 compliant FRUs have an FRU Device ID. A Participant is an ANSI/VITA 46.11 FRU which is not a RTM Device.

T2-RUL-1050: A Remote Participant **shall** have an FRU Device ID of greater than 0.

T2-OBS-0330: sections 4.1.1 and 5.1.1 of ANSI/VITA 46.11 define the basic requirements for communicating over the IPMB. This includes IPMB interface and IPMI message timing specification definitions.

5.2.4.1.1 MPP Message Header

TABLE 5-7 presents the message header used for all MPP Messages. The MPP Message Header Format defines bytes and fields used to communicate between the Manager and Participants.

Table 5-7 – MPP Message Header Format

Bytes:	**Byte 0**	**Byte 1**		**Byte 2**	**Byte 3**	**Byte 4**		**Byte 5**		**…**	**Byte n**
# of bits	8 bits	2 bits	6 bits	8 bits	8 bits	2 bits	6 bits	8 bits	8 bits		8 bits
Field Name	rsSA	rsLUN	NetFn	Csum 1	rqSA	rqLUN	rqSeq	Cmd	Data 0	…	Csum 2

5.2.4.1.2 MPP Message Header requirements

T2-RUL-1120: A MPP Message, Command, and Request **shall** only contain Field names and the allocated bytes as specified in TABLE 5-7.

T2-RUL-1130: MPP Messages **shall** use rsSa and rsLUN fields of TABLE 5-7 as the Destination Identifier for the Communication Header.

T2-OBS-0350: rsSa is defined as the IPMB address of the Command destination.

T2-OBS-0360: rsLUN is defined as the logical unit of the Command destination.

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T2-RUL-1140: MPP Messages **shall** use NetFn and Cmd fields of TABLE 5-7 as the Unique Identifiers for the MPP Message.

T2-OBS-0370: NetFn is defined as the Network function group. This field indicates the Command set (Chassis, Bridge, Storage, etc.) to which the Command belongs. Even NetFn values indicates Commands, Odd NetFn values indicates *Responses*.

T2-OBS-0380: Cmd field is defined as the Command to execute.

T2-RUL-1150: MPP Messages **shall** use rqSa and rqLUN fields of TABLE 5-7 as the Source Identifier for the Communication Header.

T2-OBS-0390: rqSA is defined as the IPMB source of the Command.

T2-OBS-0400: rqLUN is defined as the logical unit of the IPMB address that is the source of the Command.

T2-OBS-0410: rqSeq is defined as the sequence number of the Command/Response pair.

T2-RUL-1160: MPP Messages **shall** use CSUM1 and CSUM2 fields of TABLE 5-7 to store the calculated checksum data.

T2-RUL-1180: Any MPP Message **shall** set Cmd field of TABLE 5-7 to store the MPP Defined Message Command ID.

T2-RUL-1190: Any MPP Message **shall** set rqSeq field of TABLE 5-7 to store the sequence of Command/Response pair of the MPP Message.

T2-OBS-0420: Csum1 is defined as the two's complement of the sum of the bytes 0 and 1 of the message.

T2-OBS-0430: Csum2 is defined as the two's complement of the sum of bytes 3 to the byte before Csum2 of the message.

5.3 Hardware

HOST standardizes hardware components so that each HOST hardware component can interface with another HOST hardware component. The different hardware components that are standardized are the Modules, Transmission Interfaces routed between Modules, and Enclosures. The HOST Components section contains the Form Factor and other mechanically oriented requirements for different hardware components, while the sections preceding it contain the electrically oriented requirements for different hardware components.

5.3.1 HOST Transmission Interfaces

The HOST Architecture establishes five Transmission Interfaces that facilitate logical and physical connectivity within the system. Each Transmission Interface, except for the SIOTI and EIOTI, contains elements of one or more planes defined in the ANSI/VITA 65.0 multi-plane architecture. This Tier 2 Core Technology Standard defines how the ANSI/VITA 65.0 multi-plane architecture is applied to the HOST Transmission Interfaces in 6U and 3U systems. These Interfaces are:

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- **System Communications** - The SCTI utilizes the Data Plane, the UTP Control Plane, and the Expansion Plane (for 6U Components). 3U does not utilize the Expansion Plane; refer to SLT3-PAY-2F2U-HOST.
- **Chassis Management** - The CMTI utilizes the ANSI/VITA 65.0 Utility Plane with the additional requirements of ANSI/VITA 46.11 for management communications. The ANSI/VITA 65.0 Control Plane may also be utilized for chassis management communications.
- **System I/O** - The SIOTI is an I/O routing layer that utilizes the ANSI/VITA 65.0 User Defined I/O.
- **External I/O** - The *External I/O Transmission Interface* (EIOTI) for this HOST Tier 2 Core Technology Standard includes the connectors used to bring the system I/O signals off the Backplane, the connectors located on a front or rear panel, and any cables, connectors, and/or circuitry in between.
- **System Power Distribution** - The SPDI will use the power distribution portions of the ANSI/VITA 46.0 and ANSI/VITA 65.0 Utility Plane with input/output power interfaces as defined by ANSI/VITA 62.0 for modular power supplies and the requirements of the EIOTI contained in this document.

The HOST Tier 2 Transmission Interface configuration is shown in FIGURE 5-5.

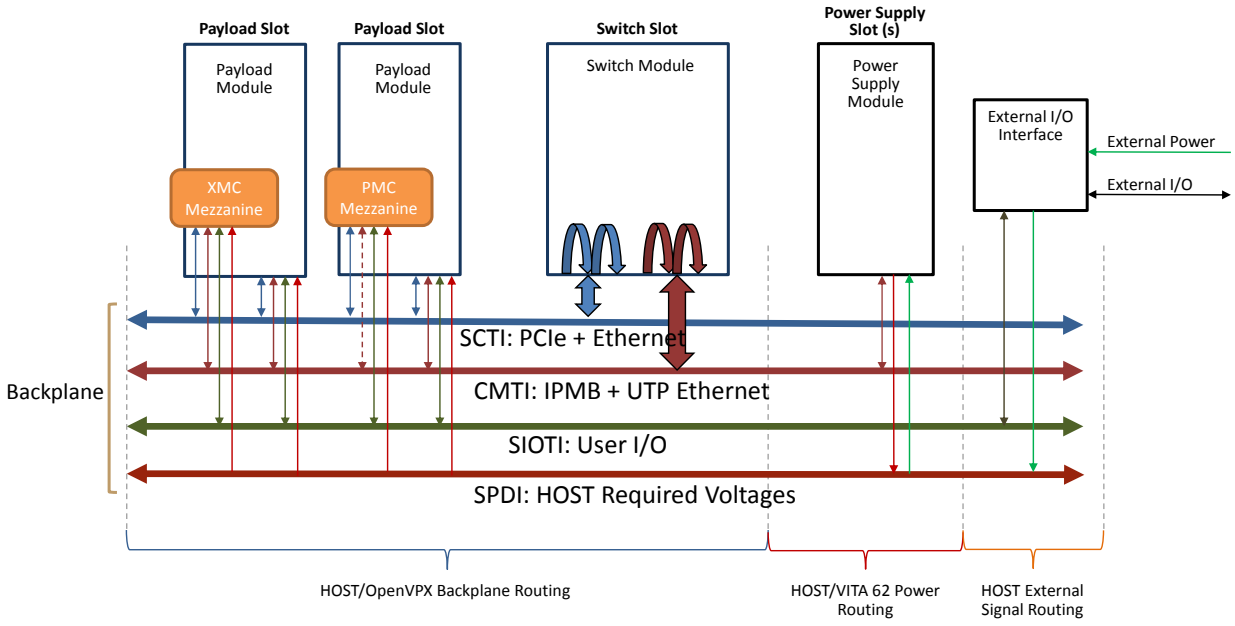

Figure 5-5 – HOST Tier 2 Transmission Interface Configuration

5.3.1.1 Common Transmission Interface Requirements

T2-RUL-2340: Backplanes **shall** implement the requirements of ANSI/VITA 65.0, section 7.2 through 7.4 (Common to 6U and 3U — *Backplane Profiles*).

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T2-RUL-2390: Backplanes **shall** prohibit the use of OpenVPX Rear Transition Modules (RTMs) for Transmission Interfaces.

5.3.1.2 System Communications Transmission Interface Requirements

The HOST SCTI is implemented in hardware using OpenVPX switched fabric Backplane and PMC/XMC mezzanine technologies. The majority of requirements for SCTI implementations will come from the electrical and mechanical requirements of ANSI/VITA 65.0 (OpenVPX System Specification) for Backplanes. The SCTI functionality is performed by the OpenVPX Data Plane and Expansion Plane (for 6U only) high-speed serial interconnects. Functionality is extended to Mezzanine Modules through PMC/XMC data bridges. The OpenVPX Data Plane transmits low-latency, high-bandwidth system data between modules utilizing Ethernet or PCI Express (PCIe). The OpenVPX Data Plane is typically a centralized switched network utilizing one or more switches. The switch, or switches, are classified as being part of the SCTI. In the case of 6U, the Expansion Plane protocol is PCIe and is typically used for communication between adjunct Modules and not through a Switch Module, though the HOST Standard does not limit the Expansion Plane to only be used in this manner. Mezzanine Module communications paths are also included as part of the SCTI. Mezzanine communications paths will sometimes include a bridge on the HOST Plug-In Module that translates PMC communications to the local bus of the Plug-In Module (usually PCI Express). In cases where resources are co-located in hardware, the physical SCTI layers may be unneeded, leaving the SCTI logical communications to be performed completely within the hardware abstraction software layers.

5.3.1.2.1 Common System Communications Interface Requirements

T2-RUL-2930: The SCTI hardware components **shall** be defined as:

1. The Data Plane portion of an OpenVPX Backplane
2. The UTPs of the Control Plane portion of an OpenVPX Backplane
3. OpenVPX conformant Plug-In network switches

T2-OBS-0640: The SCTI is physically composed of an OpenVPX Backplane and Plug-In switch module(s) that perform the network packet switching.

5.3.1.2.2 Mezzanine System Communications Interface Requirements

T2-RUL-2990: The SCTI **shall** include Payload Module's communications bridges to convert the SCTI protocols located on the Backplane to the appropriate PMC/XMC communications protocols for Mezzanine Modules.

T2-RUL-3000: If Payload Modules have Mezzanine Module sites, SCTI communications bridges **shall** be located on the Payload Modules.

T2-PER-0180: Payload Modules that have attached mezzanines **may** be carrier boards where their only purpose is to support Mezzanine Modules.

T2-RUL-3010: The SCTI, as bridged to mezzanine slots, **shall** conform to the communications requirements of one of the following mezzanine card standards:

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1. IEEE Std. 1386.1 Standard for PCI Mezzanine Cards
2. ANSI/VITA 42 Standards for Switched Mezzanine Cards

T2-RUL-3020: Requirements for SCTI mezzanine communications **shall** be applied using the following order of precedence:

1. Requirements of this Tier 2 HOST Standard (including additions or exclusions to PMC/XMC standards).
2. Mezzanine Module requirements of IEEE 1386.1 and ANSI/VITA 42.0 for PMCs and XMCs respectively.

T2-RUL-3030: The SCTI as bridged to PMC Mezzanine Modules **shall** conform to PMC 64-bit 33/66MHz PCI V2.3 communications standard.

T2-RUL-3040: The SCTI as bridged to XMC Mezzanine Modules **shall** conform to ANSI/VITA 42.3, American National Standard for XMC PCI Express Protocol Layer Standard.

T2-OBS-0650: XMC Mezzanine Modules that conform to parallel and Serial RapidIO protocols are not supported in this standard.

5.3.1.2.3 6U System Communications Transmission Interface Requirements

T2-RUL-3041: The 6U SCTI hardware components **shall** also be defined as the Expansion Plane portion of an OpenVPX Backplane.

5.3.1.3 System I/O Transmission Interface Requirements

The SIOTI is implemented as internal routing on the OpenVPX Backplane and connects the EIOTI with the User Defined pins of the HOST Plug-In Module slots. The SIOTI is intended for routing external I/O to and from modules and cannot be used for custom, inter-module communications that circumvent the chassis management, modularity, and openness of HOST.

5.3.1.3.1 Common System I/O Interface Requirements

T2-RUL-3050: The SIOTI hardware components **shall** be implemented as internal routing on the OpenVPX Backplane.

T2-PER-0185: Optical Signals **may** be implemented over an optical fiber cable going directly from the Platform to a Module Slot containing an ANSI/VITA 66.0 compliant connector.

T2-RUL-3080: All user defined pins, as defined in the HOST Module Slot Profiles of SECTION 5.1.1.1.2.1 and SECTION 5.1.1.1.3.1, **shall** be transmitted exclusively via the SIOTI.

T2-OBS-0660: The SIOTI connector pinouts with respect to mezzanine interfaces are referenced in SECTION 5.1.1 and SECTION 5.1.2.

5.3.1.3.2 Backplane System I/O Interface Requirements

T2-RUL-3090: The SIOTI Backplane routing **shall** provide connectivity between the SIOTI and the EIOTI.

T2-OBS-0670: The user defined signals transmitted by the SIOTI are generically defined by the Slot and Module Profiles.

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5.3.1.4 External I/O Transmission Interface Requirements

This Tier 2 HOST Standard broadly defines the Backplane mechanical and electrical connector interface portions of the EIOTI giving it the flexibility to meet the mechanical and electrical constraints of a target-system. This Tier 2 HOST Standard does not define the target-system interface panel mechanical and electrical portions of the EIOTI as that is defined by the target-system requirements.

The EIOTI Interconnect Diagram is shown in FIGURE 5-6.

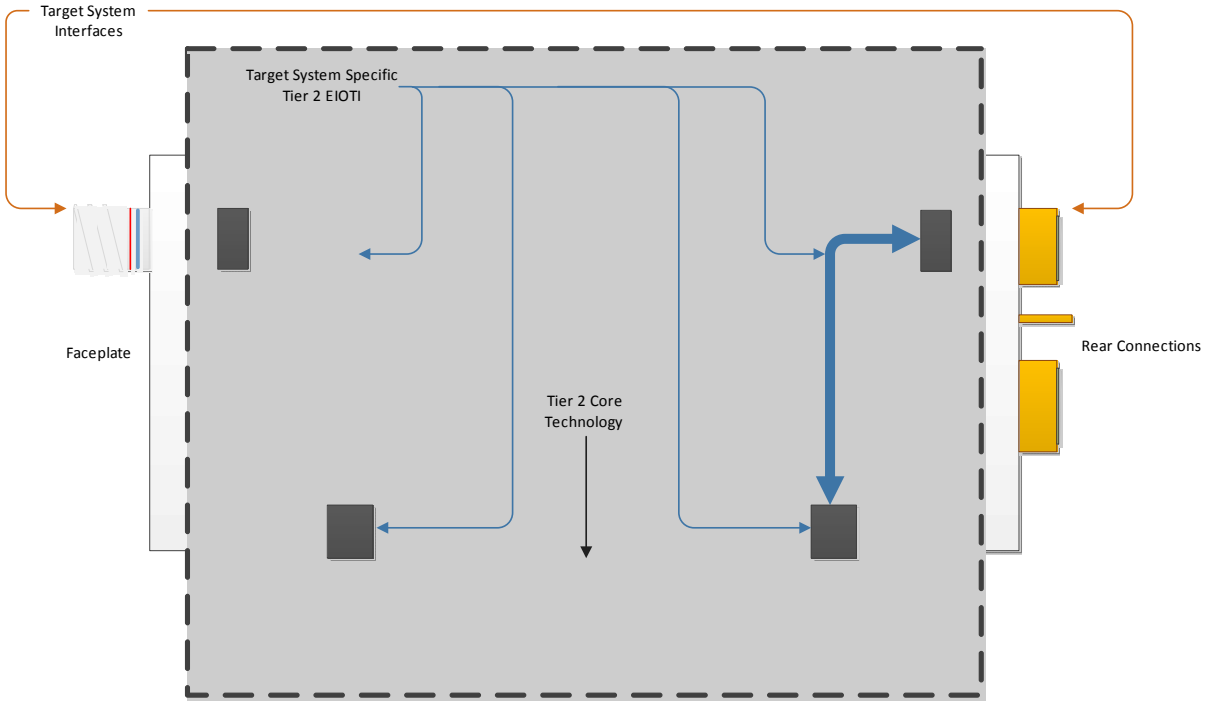

Figure 5-6 – HOST EIOTI Interconnect Diagram

T2-REC-0035: The EIOTI **should** be a modular unit that can be disconnected from the OpenVPX Backplane.

T2-OBS-0680: Modular EIOTI units facilitate HOST implementation migration and Target System lifecycle upgradeability and serviceability requirements.

T2-RUL-3120: The EIOTI **shall** provide connectivity between the external I/O at an enclosure-level panel interface and the SIOTI at a Backplane interface.

T2-RUL-3130: The EIOTI **shall** provide connectivity between the target-system input power at an enclosure-level panel interface and the SPDI at a Backplane interface.

T2-OBS-0690: The mechanical requirements for EIOTI modules are addressed in SECTION 5.3.2.

T2-RUL-3140: All external panel I/O signals **shall** pass through the EIOTI Backplane connector(s) before going to any HOST Module.

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T2-PER-0195: Optical Signals over a fiber cable **may** bypass the EIOTI Backplane connector(s) and go directly from the Platform to a Module Slot containing an ANSI/VITA 66.0 compliant connector.

T2-OBS-0700: External front or rear panel chassis I/O signals includes video and power.

T2-RUL-3150: All SIOTI Interface signals **shall** pass through the EIOTI Backplane connector(s) before going to any external front or rear panel chassis I/O connectors.

T2-OBS-0705: When connecting the front/rear panel connectors directly to the Backplane, those connectors are considered the EIOTI Backplane connectors.

T2-RUL-3170: All EIOTI Backplane connectors **shall** be commercially available connectors that can be procured by any vendor without prior authorization from any source (e.g. a commercial part governed by a source control drawing).

T2-RUL-3180: The EIOTI **shall** provide a path for connecting chassis ground to the SPDI at the Backplane in support of ANSI/VITA 65.0, section 3.2.3, Safety Ground.

5.3.1.5 Chassis Management Transmission Interface Requirements

The CMTI is implemented in hardware using OpenVPX Backplane technology. The majority of requirements for CMTI implementations will come from the electrical and mechanical requirements of ANSI/VITA 65.0 (OpenVPX System Specification) for Backplanes. CMTI functionality is performed by portions of the OpenVPX Control Plane, the OpenVPX Utility Plane and the OpenVPX Management Plane implementing ANSI/VITA 46.11. The OpenVPX Control Plane may be used for transmission of MPP messages and large data transfers such as OFP loading. The OpenVPX Utility Plane includes power distribution functions and common control/status signals. The CMTI only includes the control/status functions of the OpenVPX Utility Plane. The OpenVPX Management Plane is implemented using the IPMB, where the Backplane contains the bus link and Plug-In Modules contain a Participant.

5.3.1.5.1 Common Chassis Management Transmission Interface Requirements

T2-RUL-3190: The CMTI hardware components **shall** be implemented utilizing:

1. The Backplane-routed control and status portions of the OpenVPX Utility Plane
2. The IPMB OpenVPX Management Plane
3. The OpenVPX Control Plane

T2-RUL-3270: Backplanes **shall** implement a single, 2.49K Ohm, +/- 1%, pull-up resistor from each CMTI IPMB signal to the 3.3V Auxiliary voltage rail.

T2-OBS-0750: The single pull-up resistor supersedes ANSI/VITA 46.0 Rule 7-1, requiring spare resistors for both single-ended and differential termination schemes.

T2-RUL-3280: HOST Modules **shall** prohibit the implementation of pull-up resistors on the CMTI IPMB signals.

T2-OBS-0760: The rule against HOST Modules having pull-up resistors on the IPMB is a clarification of ANSI/VITA 46.11 Rule 9.2.3-2.

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T2-RUL-3290: HOST Modules containing resources to drive the Utility Plane REF_CLK+/- signals **shall** provide a mechanism to permit *Application Software* or system management to reassign the identity of the SYS_CON module, regardless of the logic level of the Backplane SYS_CON* contact, in order to control these signal drivers once the Backplane power rails are all at minimum operating voltages as defined in ANSI/VITA 46.0, section 4.8.12.4.

T2-OBS-0765: The SYS_CON module identity reassignment was a Recommendation 3.4.1-1 in ANSI/VITA 65.0.

T2-RUL-3291: The NVMRO portion of the CMTI **shall** conform to the low current open-drain signal specifications of ANSI/VITA 65.0, section 3.3.1.

T2-RUL-3300: The SYSRESET* portion of the CMTI **shall** conform to the high current open-drain signal specifications of ANSI/VITA 65.0, section 3.3.3 (High Current Open-Drain).

T2-RUL-3310: Plug-In Modules receiving SYSRESET* as an input **shall** be able to register a valid low for any pulse length of 10ms or longer.

T2-RUL-3320: Payload Modules **shall** make SYSRESET* available to any Mezzanine Module connector that has SM1 and SM0 available per ANSI/VITA 65.0 Recommendation 3.4.2.1-1.

T2-RUL-3323: The Load_Enable* portion of the CMTI **shall** conform to the low current open-drain signal specifications of ANSI/VITA 65.0, section 3.3.1.

T2-RUL-3325: The Data_Purge* portion of the CMTI **shall** conform to the low current open-drain signal specifications of ANSI/VITA 65.0, section 3.3.1.

T2-OBS-0766: If the Backplane is routing the Load Enable, User Mode[2..0], or Data Purge signals it will need a pull up resistor to 3.3V auxiliary.

T2-RUL-3321: The Backplane **shall** provide a method for optionally pulling the SYS_CON* signal low for all Payload and Switch Slots.

T2-RUL-3322: GAP* and GA[4:0] **shall** be wired to indicate physical slot numbers, with the numbers going from 1 thru N, where N is the number of slots.

T2-RUL-3330: Plug-In Modules **shall** receive a unique Site Number that is based upon the Module's ANSI/VITA 65.0, section 3.4.6, Geographic Address.

T2-OBS-0770: ANSI/VITA 65.0, section 3.4.6, Geographic Address Field, specifies how geographical addressing is accomplished for OpenVPX modules.

T2-OBS- 0775: It is recommended in ANSI/VITA 46.0 that JTAG pins not be bussed on Backplanes.

T2-OBS-0790: ANSI/VITA 65.0, section 3.4.7, JTAG Port, specifies that each P0/J0 connector must support the JTAG signal assignment established in ANSI/VITA 46.0. The JTAG port is designated for single-card use outside of the Target System only. For example, it can be used for single-card manufacturing, programming, or debug purposes.

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T2-RUL-3370: The Control Plane as defined in SECTION 5.1.1.1 and SECTION 5.1.1.3 **shall** be included as part of the CMTI.

T2-RUL-3371: If a Payload Module has an XMC Mezzanine site, the Payload Module **shall** route the ANSI/VITA 42.0 defined I2C connections from the XMC Mezzanine Site to the Participant of the Payload Module.

T2-OBS-0792: XMC Mezzanine Modules conform to the requirements for supporting the CMTI through the Participant located on the parent Payload Modules. An example is illustrated in FIGURE 5-7.

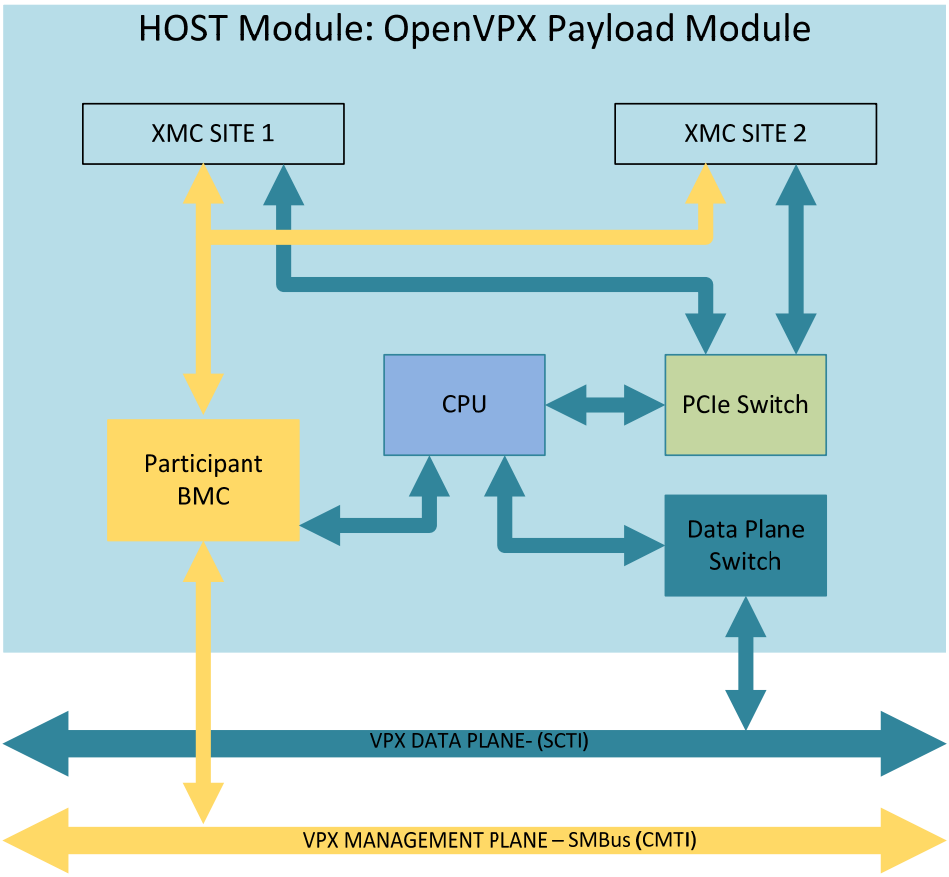

Figure 5-7 – Example HOST Payload Module XMC Mezzanine CMTI Configuration

T2-OBS-0793: PMC Mezzanine Modules conform to the requirements for supporting the CMTI through the parent Payload Module utilizing Remote Participant Proxy software components. An example is illustrated in FIGURE 5-8.

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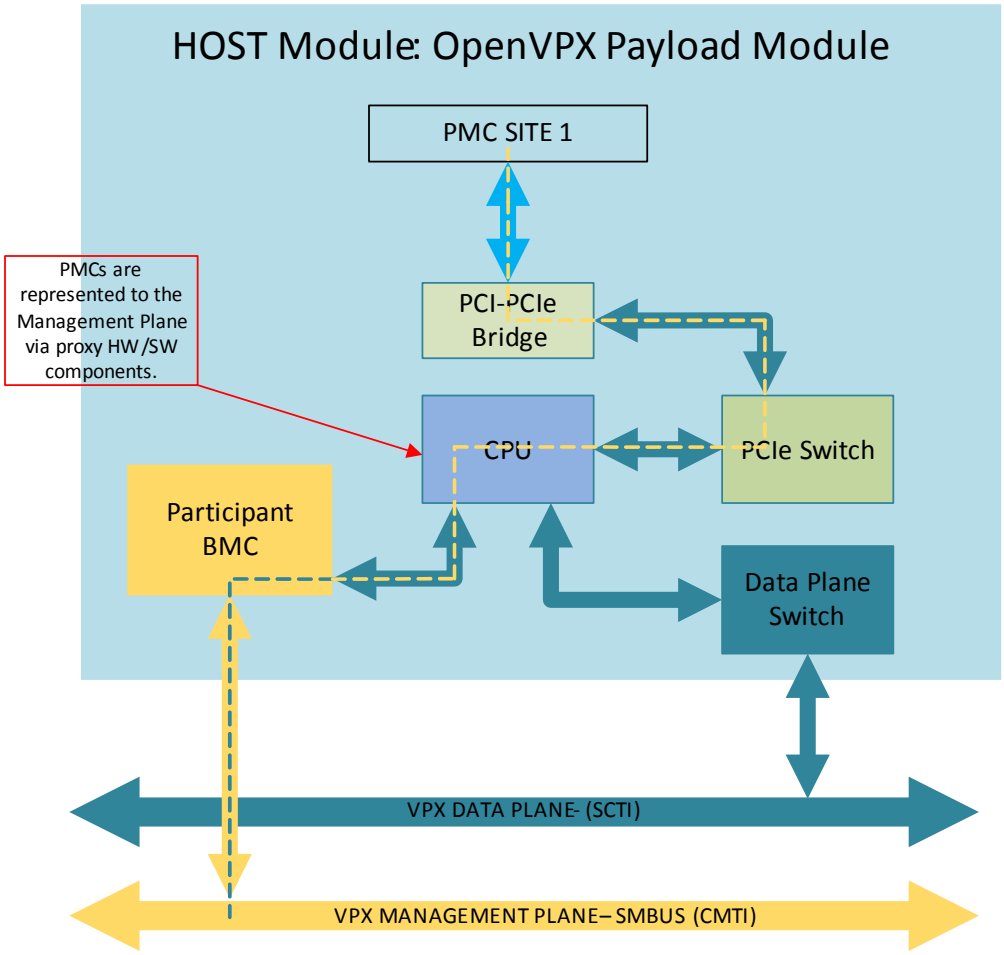

Figure 5-8 – Example HOST Payload Module PMC Mezzanine CMTI Configuration

5.3.1.5.1.1 Utility Plane

T2-RUL-3391: Payload and Switch Modules **shall** conform to the OpenVPX Utility Plane signals for P0/J0 as described in ANSI/VITA 65.0, Table 3.7-1 and 3.7-2.

T2-RUL-3392: Payload and Switch Modules **shall** conform to the OpenVPX Utility Plane signals for P1/J1 as shown in TABLE 5-8 and TABLE 5-9.

Table 5-9

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Table 5-8 – Utility Plane Signals on P1

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Data_Purge*						
2	GND						
3	P1-VBAT						
4	GND						
5	SYS_CON*						
6	GND						
7	Reserved						
8	GND						
9	UD						
10	GND						
11	UD						
12	GND						
13	Load_Enable*						
14	GND						
15	MaskableReset*						
16	GND						

Table 5-9 – Utility Plane Signals on J1

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data_Purge*								
2	GND								
3	P1-VBAT								
4	GND								
5	SYS_CON*								
6	GND								
7	Reserved								
8	GND								
9	UD								
10	GND								
11	UD								
12	GND								
13	Load_Enable*								
14	GND								
15	MaskableReset*								
16	GND								

Note: Signals marked with an * are active, logic 1, at the less positive value level of its allowable range.

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5.3.1.5.1.1.1 **Data Purge***

The Data Purge function on HOST Backplanes utilizes a common open-drain backplane signal (Data_Purge*) on pin G1 of the P1 connector (contact i13 on the backplane connector). A Module that has Manager capability is required to have the ability to monitor the Data_Purge* signal to determine if the chassis is to perform a data purge as defined by the Platform requirements. This standard does not impose requirements on the source of Data_Purge* signal.

T2-RUL-3393: The Manager **shall** have the ability to monitor the Data_Purge* signal to determine if the chassis is to transition to Data Purge Chassis Mode.

T2-REC-0040: A slot that is not capable of being a Manager **should** mark the Data_Purge* pin as Reserved.

T2-RUL-3394: The Data_Purge* signal **shall** have a minimum active low pulse width of 10ms.

T2-RUL-3395: The received Data_Purge* signal **shall** be debounced prior to application to internal circuitry.

5.3.1.5.1.1.2 **Load Enable***

The active low open-drain Load_Enable* signal is used by the Platform to indicate when the chassis is to go into the Load/Verify Chassis Mode. A Module that has Manager capability is required to have the ability to monitor the Load_Enable* signal to determine if the chassis is to transition to the Load/Verify Chassis Mode. This standard does not impose requirements on the source of the Load_Enable* signal.

T2-RUL-3397: The Manager **shall** have the ability to monitor the Load_Enable* signal to determine if the chassis is to transition to Load/Verify Chassis Mode.

T2-REC-0041: A Payload Module that is not capable of being a Manager **should** mark the Load_Enable* pin as Reserved.

5.3.1.5.2 **6U Chassis Management Interface Requirements**

T2-RUL-3220: The 6U hardware components implementing the IPMB Management Plane **shall** conform to the electrical requirements of ANSI/VITA 46.11 as applied to 6U OpenVPX implementations except where specified herein.

T2-RUL-3250: The 6U CMTI electrical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 6U OpenVPX implementations excluding ANSI/VITA 65.0, section 3.2, Power Distribution.

T2-RUL-3260: The 6U CMTI mechanical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 6U OpenVPX implementations excluding ANSI/VITA 65.0, section 3.2, Power Distribution.

T2-OBS-0710: HOST power distribution is accomplished with the SPDI.

T2-OBS-0730: ANSI/VITA 65.0, section 3.3, Electrical Standards for Drivers and Receivers, specifies the electrical parameters for the OpenVPX Utility Plane.

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T2-OBS-0740: ANSI/VITA 65.0, section 3.4, System Control Signals, defines the OpenVPX Utility Plane signals and their functionality.

5.3.1.5.3 3U Chassis Management Interface Requirements

T2-RUL-3261: The 3U hardware components implementing the IPMB Management Plane **shall** conform to the electrical requirements of ANSI/VITA 46.11 as applied to 3U OpenVPX implementations except where specified herein.

T2-RUL-3262: The 3U CMTI electrical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 3U OpenVPX implementations excluding ANSI/VITA 65.0, section 3.2, Power Distribution.

T2-RUL-3263: The 3U CMTI mechanical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 3U OpenVPX implementations excluding ANSI/VITA 65.0, section 3.2, Power Distribution.

T2-OBS-0741: HOST power distribution is accomplished with the SPDI.

T2-OBS-0742: ANSI/VITA 65.0, section 3.3, Electrical Standards for Drivers and Receivers, specifies the electrical parameters for the OpenVPX Utility Plane.

T2-OBS-0743: ANSI/VITA 65.0, section 3.4, System Control Signals, defines the OpenVPX Utility Plane signals and their functionality.

T2-OBS-0744: 3U Power Supply Modules only have GA[1:0] due to pin count. If it is desired that the PSM be higher than slot 4, offset logic will need to be implemented. For example, a specific Backplane power supplies start at logical slot 6, for 3U PSMs GA1 GND and GA0 Open would mean logical slot 7.

5.3.1.6 System Power Distribution Interface Requirements

The HOST SPDI primary function is distributing power to Plug-In Modules. The SPDI distributes defined voltages to each payload and switch slot on the Backplane via the OpenVPX Utility Plane. The ANSI\VITA 65.0, signals VS1, VS2, VS3, 3.3V_AUX, and +/-12V_AUX of the OpenVPX Utility Plane make up the SPDI. The SPDI is also responsible for transporting prime power to the *Power Supply Resource* (PSR) and intermediate power between PSR stages and/or to Energy Storage Modules described in SECTION 5.1.1.2.

5.3.1.6.1 Common System Power Distribution Interface Requirements

T2-RUL-3420: The SPDI **shall** conform to the Backplane requirements of ANSI/VITA 65.0, section 3.2 except where specified herein.

T2-RUL-3430: For HOST Payload and Switch Slots, the SPDI **shall** exclusively support the Power Distribution portion of the OpenVPX Utility Plane.

T2-RUL-3450: The SPDI **shall** conform to the 12V for the High Voltage Power Input requirements of ANSI/VITA 46.0, section 4.8.1.1.3.

T2-RUL-2360: Backplanes **shall** size Vs1 to be able to distribute at least 14 A per slot. Refer to connector current load limits in ANSI/VITA 46.0, section 4.8.1.

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T2-RUL-2365: Backplanes **shall** size Vs2 to be able to distribute at least 14A per slot. Refer to connector current load limits in ANSI/VITA 46.0, section 4.8.1.

T2-RUL-2375: Backplanes **shall** have a 4.7K pull-up on the PSM slot's FAIL* signal, as is recommended in Observation 4.6.3.7-1 of ANSI/VITA 62.0.

T2-RUL-3460: If a Payload Module supports a PMC site, a Payload Module **shall** route the SPDI to the appropriate PMC connectors per IEEE 1386.1.

T2-RUL-3465: If a Payload Module supports a XMC site, a Payload Module **shall** route the SPDI to the appropriate XMC connectors per ANSI/VITA 42.0.

T2-OBS-0820: Due to the site profile provided for PMCs, a Payload Module implementing that site profile will need to route the SPDI to both the XMC and PMC connectors.

T2-RUL-3470: The SPDI **shall** conform to the requirements for Single-Stage or Two-Stage power subsystems as specified by ANSI/VITA 62.0.

T2-OBS-0830: If a subsystem requires any Energy Storage Modules then the SPDI also must support the Energy Storage Module.

T2-RUL-3480: The SPDI **shall** provide a Backplane interface connector for transmitting Platform power from the EIOTI to the SPDI.

T2-RUL-3490: The SPDI **shall** receive a chassis ground signal from the EIOTI.

5.3.1.6.2 **6U System Power Distribution Interface Requirements**

T2-RUL-3400: The SPDI for 6U component interfaces **shall** conform to the 6U Backplane electrical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-RUL-3410: The SPDI for 6U component interfaces **shall** conform to the 6U Backplane mechanical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-OBS-0810: Some sections of ANSI/VITA 62.0 and 65.0 contain requirements for air-cooled modules only. These requirements are not applicable to this Tier 2 technology.

T2-RUL-2370: Backplanes **shall** size Vs3 to be able to distribute at least 22 A per 6U slot. Refer to current load limits in ANSI/VITA 46.0, section 4.8.1.

T2-OBS-0811: The power rail sizes are the recommended minimums from ANSI/VITA 65.0, section 11.2.1.2.1.

5.3.1.6.3 **3U System Power Distribution Interface Requirements**

T2-RUL-2371: The SPDI for 3U component interfaces **shall** conform to the 3U Backplane electrical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-RUL-2372: The SPDI for 3U component interfaces **shall** conform to the 3U Backplane mechanical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

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T2-OBS-0812: Some sections of ANSI/VITA 62.0 and 65.0 contain requirements for air-cooled modules only. These requirements are not applicable to this Tier 2 technology.

T2-RUL-2373: Backplanes **shall** size Vs3 to be able to distribute at least 15 A per 3U slot. Refer to current load limits in ANSI/VITA 46.0, section 4.8.1.

T2-OBS-0813: The power rail sizes are the recommended minimums from ANSI/VITA 65.0 section 15.2.1.2.1.

5.3.2 HOST Components

A notional layout for a HOST implementation is presented in FIGURE 5-9. This figure shows a hypothetical design to provide clarification for HOST Component descriptions. Layouts for specific enclosure designs will vary.

As seen in the figures, the system for this Tier 2 technology comprises components from four categories, defined in the following sections:

- **HOST Enclosure –** The enclosure design is variable and is designed to suit the requirements of the target-system. In the following notional views, it is approximated by a standard 1 ATR enclosure, defined in ARINC 404A.
- **HOST Module –**Payload Module, Switch Module, PMC/XMC Mezzanine Module, or Power Supply Module.
- **HOST Backplane –** A physical circuit card assembly that accepts HOST Plug-In Modules and provides access to HOST Transmission Interfaces. The transmission components may also consist of discrete wires or cable assemblies serving as the connection between HOST Modules and *HOST External Interfaces*.
- **HOST External Interfaces –** External interfaces transfer signals and power between the HOST Transmission Components and the external system.

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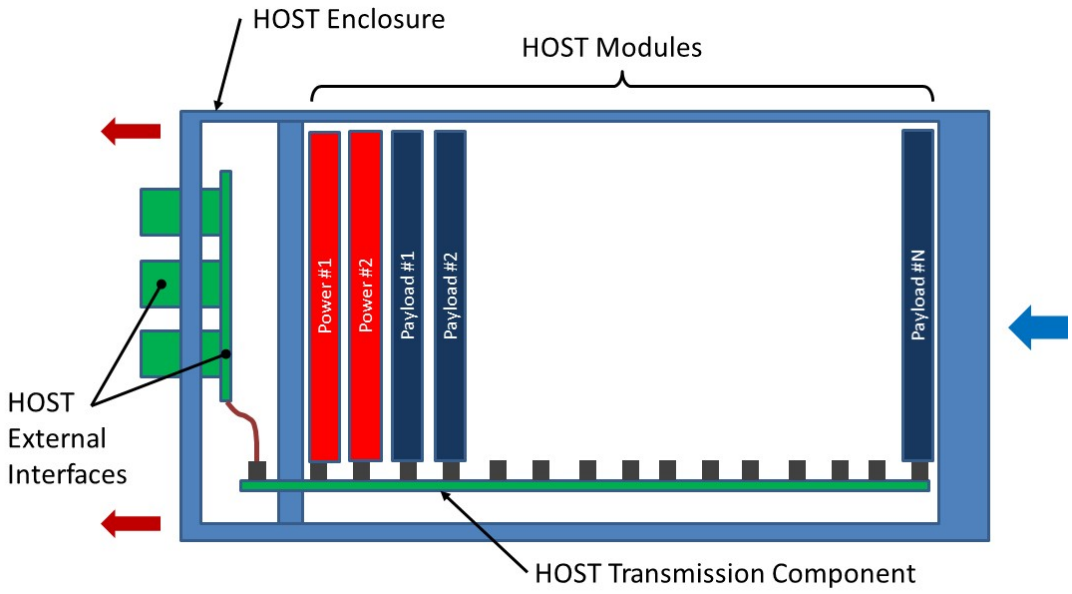

Figure 5-9 – Notional Side View of a Generic ATR Mission Computer

T2-RUL-3510: Environmental and performance tests, where applicable, **shall** be done in accordance with ANSI/VITA 47.0 per TABLE 5-10.

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Table 5-10 – Environmental and Performance Test Requirements

Environment	**ANSI/VITA 47.0 Section**
Operating Temperature	4.1
Non-Operating Temperature	4.2
Temperature Cycling	4.3
Vibration	4.4
Shock	4.5
Humidity	4.6
Altitude	4.7
Rapid Decompression	4.8
Attitude	4.9
Fungus Resistance	4.10
Electrostatic Discharge Resistance (With Optional Covers)	4.11
Corrosion Resistance	4.12

5.3.2.1 **HOST Enclosure**

5.3.2.1.1 **Form Factor**

T2-OBS-0840: External form factor requirements will be dictated by the requirements of the target-system.

T2-RUL-3520: The Payload Module region of the enclosure **shall** house Payload Modules as defined by SECTION 5.1.1.1.

T2-RUL-3530: The Switch Module region of the enclosure **shall** house Switch Modules as defined by SECTION 5.1.1.3.

T2-RUL-3540: The Power Supply Module region of the enclosure **shall** house power supply modules as defined in SECTION 5.1.1.2.

5.3.2.1.2 **Card Cage Environment and Form Factor**

T2-RUL-3550: The enclosure **shall** have rail geometry in accordance with IEEE 1101.2-1992 (R2008).

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T2-RUL-3560: The card cage rail **shall** have a pitch of 1 inch for all electronic module slots.

T2-OBS-0850: The rail geometry for 6U is further specified in FIGURE 5-10 and the rail geometry for 3U is further specified in FIGURE 5-11.

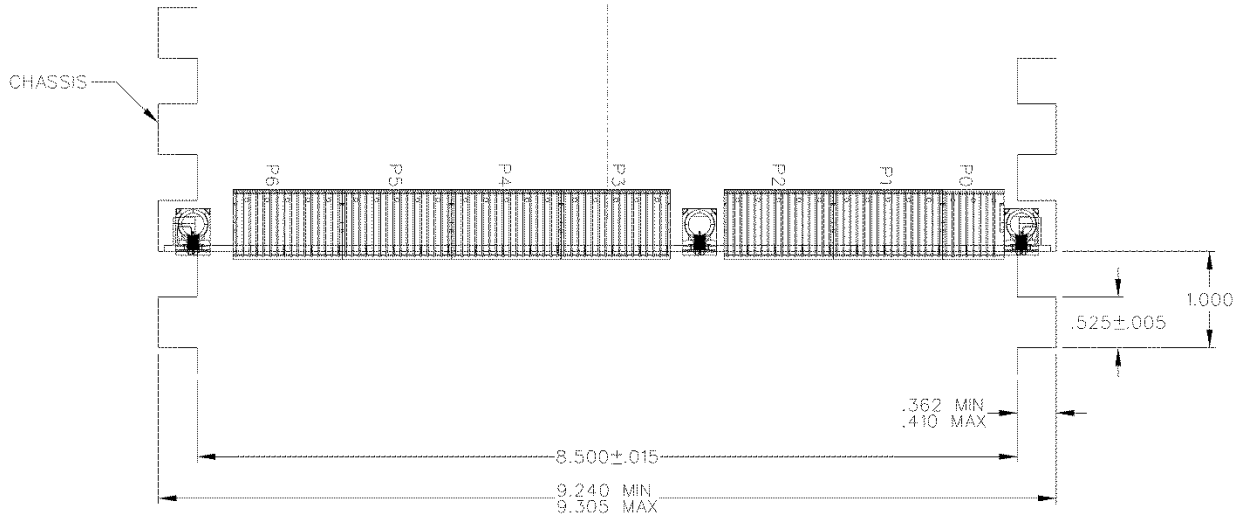

Figure 5-10 – 6U Rail Geometry

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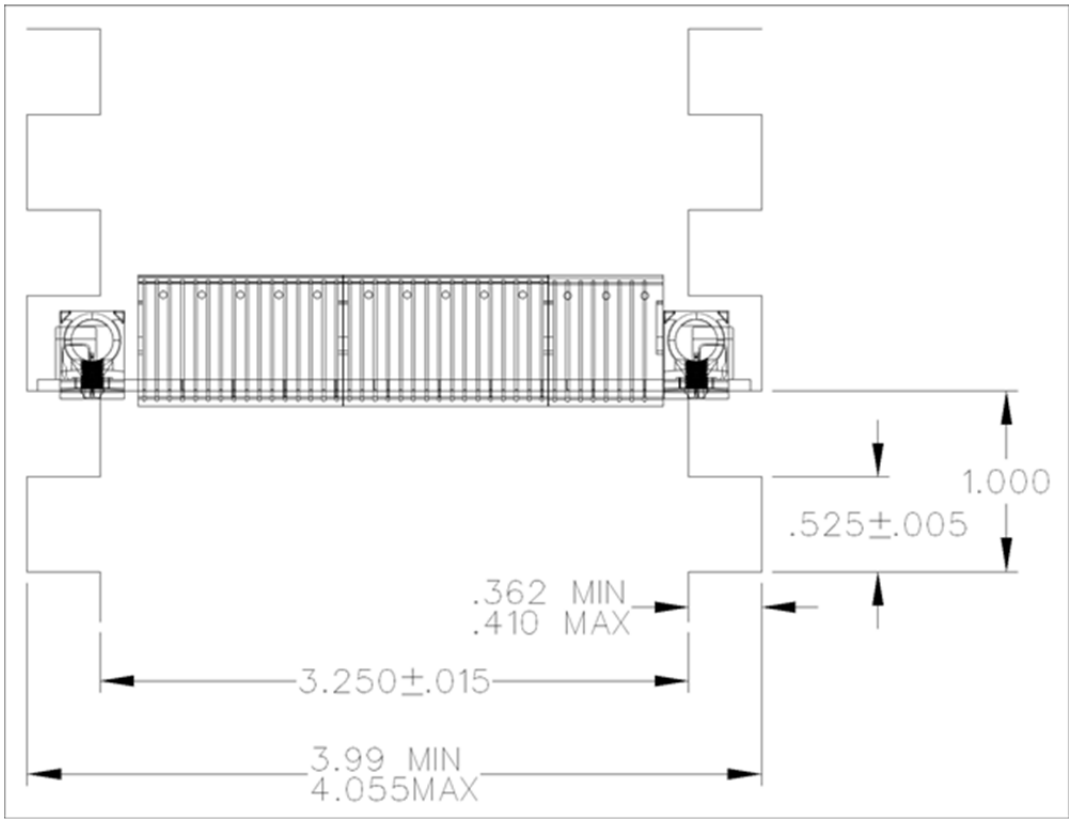

Figure 5-11 – 3U Rail Geometry

T2-RUL-3570: The card cage **shall** utilize wedgelocks as defined in ANSI/VITA 46.0, Appendix A (See FIGURE 5-12).

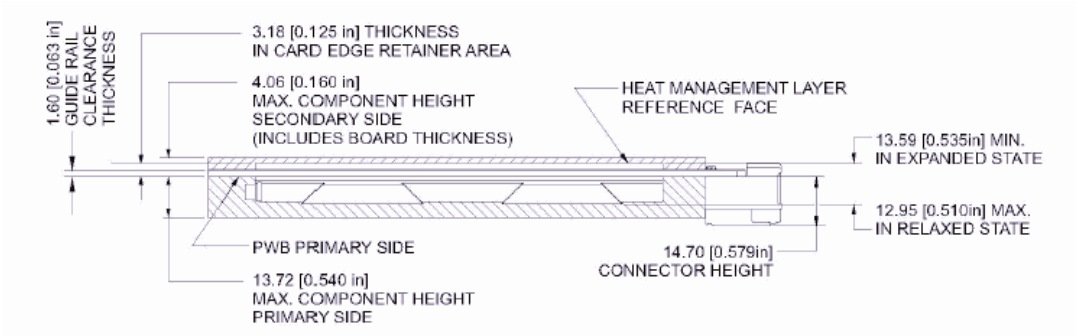

Figure 5-12 – Wedgelock Geometry

T2-RUL-3580: The enclosure card cage **shall** provide conduction cooling to the electronic modules.

T2-RUL-3590: The enclosure card cage **shall** provide a module rail temperature less than or equal to +85°C during the worst-case thermal loading with all slots filled unless otherwise specified by the target-system.

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T2-RUL-3600: The enclosure card cage **shall** provide a vibration environment equal to or better than ANSI/VITA 47.0, Vibration Class: V3.

5.3.2.1.3 **Liquid –Cooled Enclosure**

To be developed in a future revision of this standard.

5.3.2.2 **HOST Module**

The standards of this section define the module requirements for the Tier 2 Standard.

5.3.2.2.1 **Form Factor**

The form factor for standard HOST OpenVPX Payload and Switch Modules is defined in ANSI/VITA 65.0, section 4. ANSI/VITA 65.0 passes the majority of these requirements through from ANSI/VITA 46.0 and ANSI/VITA 48, which refer to standard form factors defined in IEEE 1101.1 and IEEE 1101.2. and FIGURE 5-14 show the required 6U form factors derived from these standards, and FIGURE 5-15 and FIGURE 5-16 show the required 3U form factors.

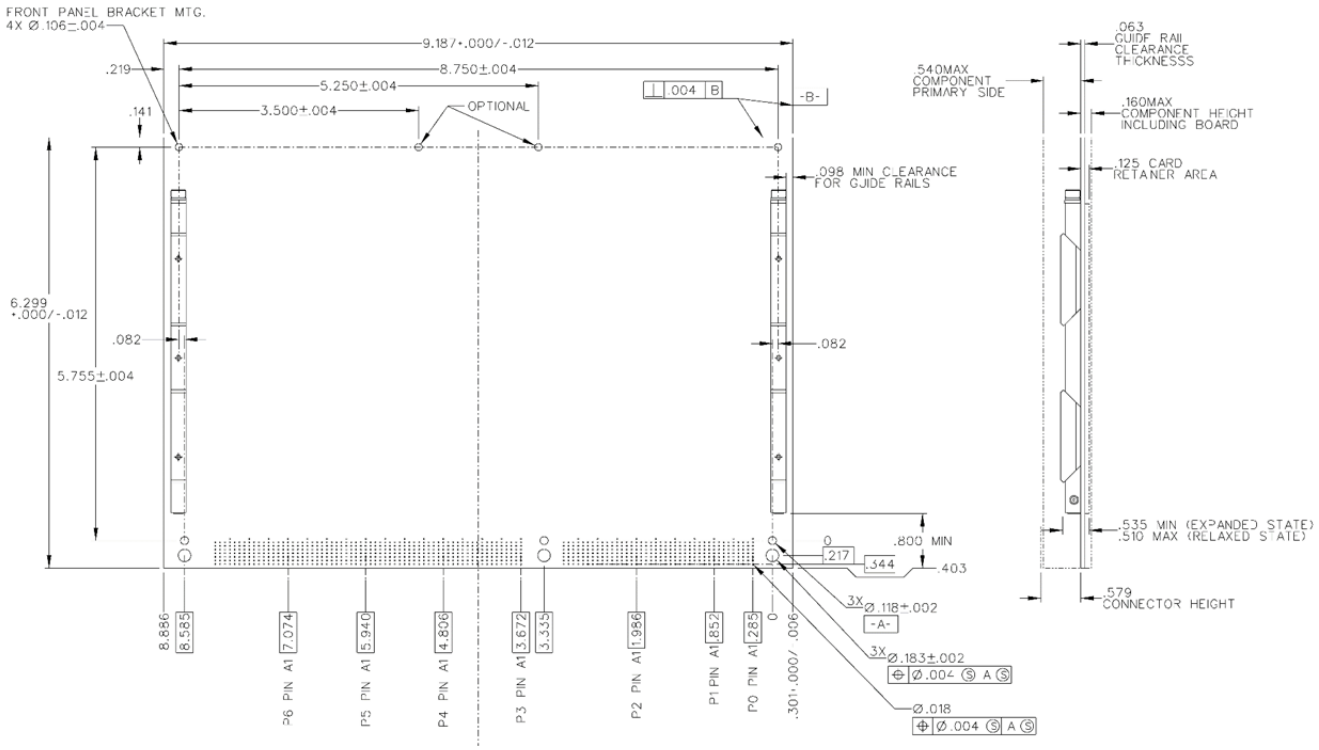

Figure 5-13 – 6U Module Layout

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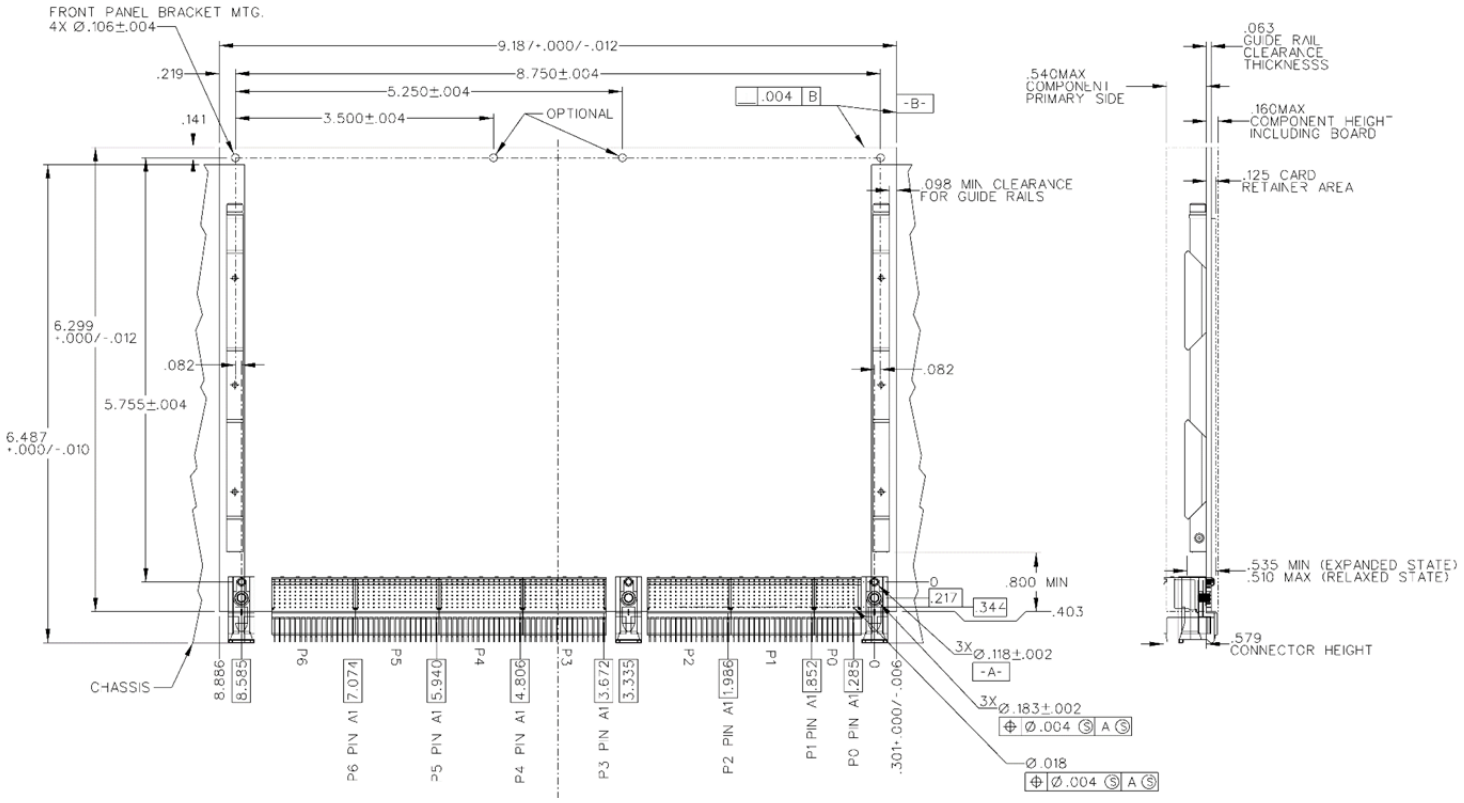

Figure 5-14 **– 6U Module Layout with Connectors and Locating Pin Sockets**

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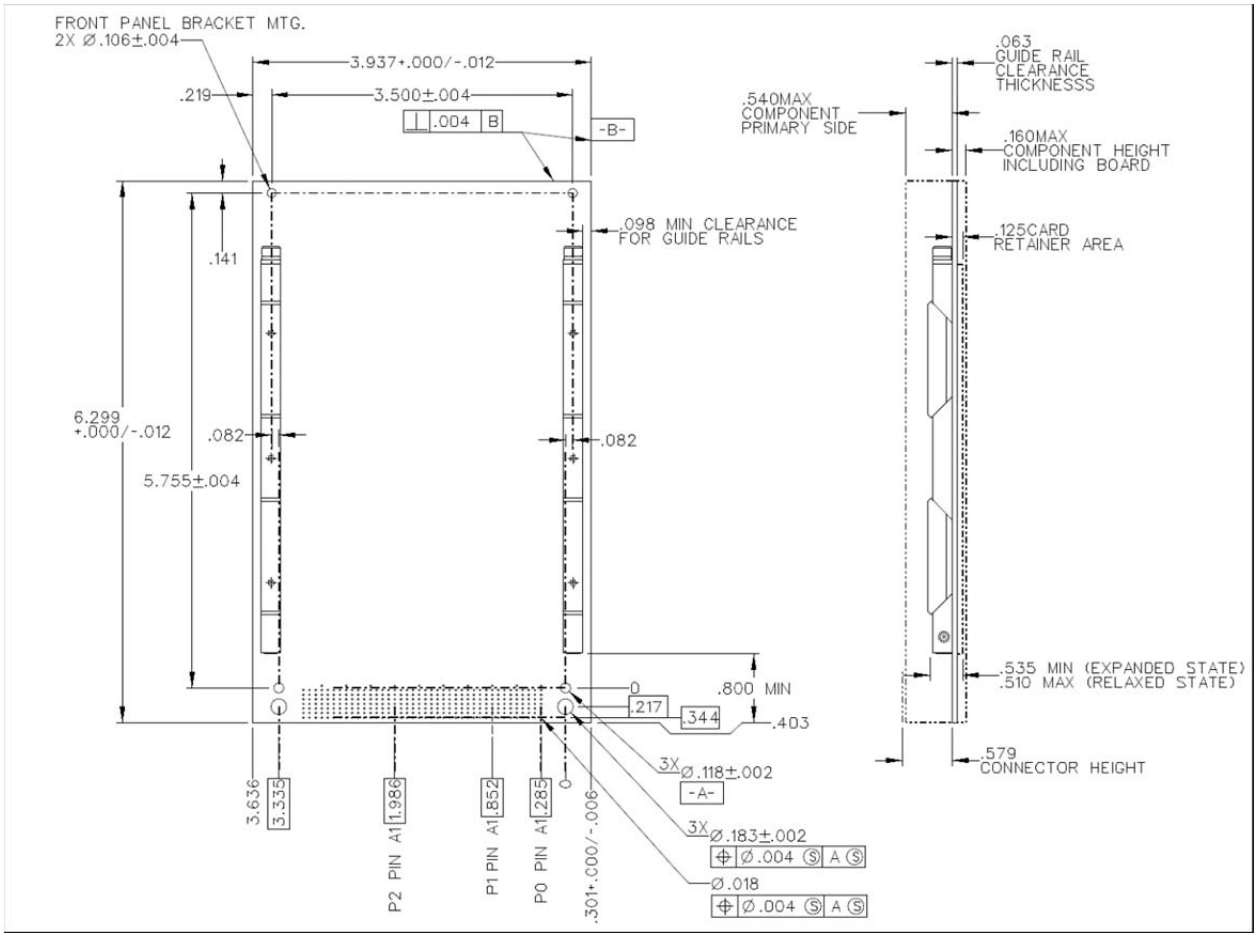

Figure 5-15 – 3U Module Layout

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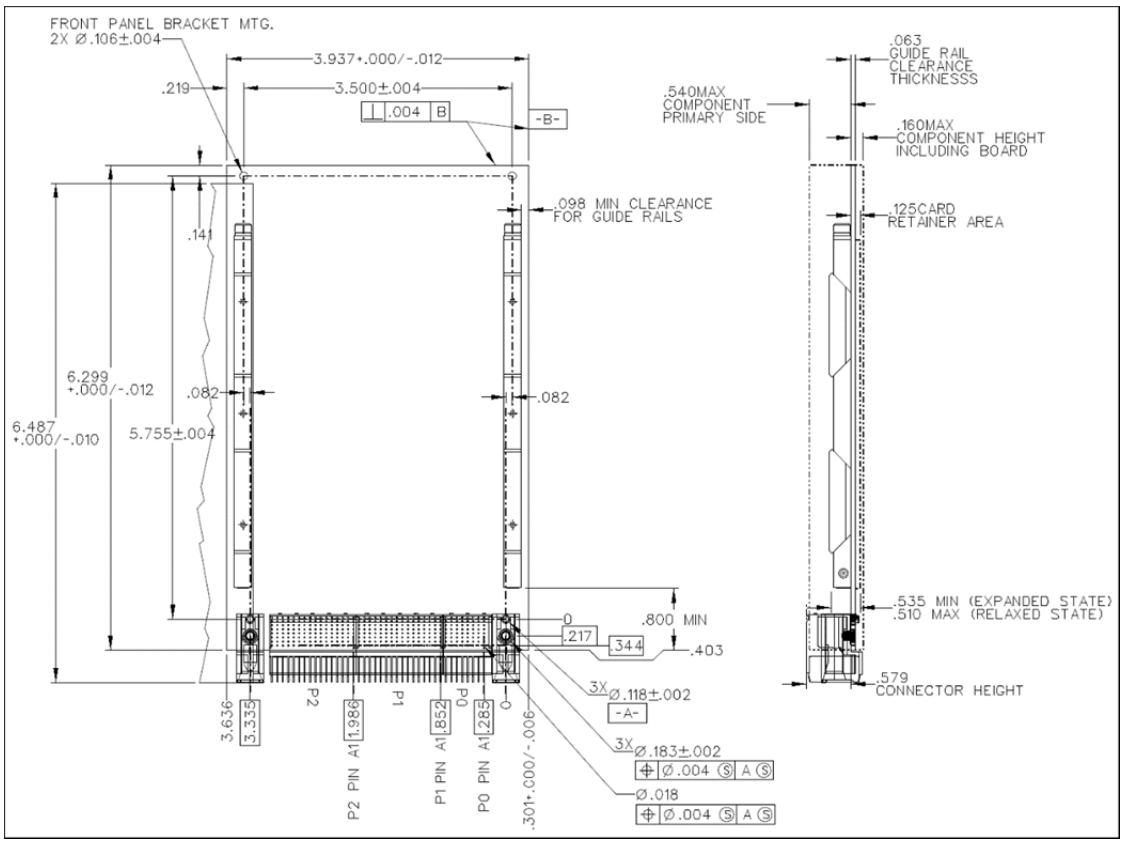

Figure 5-16 – 3U Module Layout with Connectors and Locating Pin Sockets

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T2-OBS-0860: Figure 5-13**,** FIGURE 5-14**,** FIGURE 5-15**,** and FIGURE 5-16 are derived from the requirements in ANSI/VITA 65.0. For clarification, refer to ANSI/VITA 65.0 and its parent documents.

T2-RUL-3610: Payload Modules **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
3. Requirements of ANSI/VITA 65.0 for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

T2-RUL-3620: Switch Modules **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
3. Requirements of ANSI/VITA 65.0 for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

T2-RUL-3630: PMC Mezzanine Modules **shall** adhere to form factor constraints provided in IEEE 1386-2001.

T2-RUL-3631: XMC Mezzanine Modules **shall** adhere to form factor constraints provided in ANSI/VITA 42.0.

T2-RUL-3640: Mezzanine Modules **shall** pass qualification testing while installed on the Payload Module including all hardware and accessories.

T2-OBS-0870: Mezzanine Modules may undergo preliminary testing, but it is a higher priority to characterize the effect of Mezzanine Modules on other resources.

5.3.2.2.2 Interfaces

T2-RUL-3670: Plug-In Modules **shall** use alignment-keying sockets defined in ANSI/VITA 46.0, Table 4-2.

T2-RUL-3680: Plug-In Modules **shall** use alignment keys as defined in ANSI/VITA 46.0, section 4.4.3 Plug-In Module Key.

T2-PER-0011: Plug-In Modules **may** use the Ruggedized Machined 6061 Aluminum RT2-R compatible keying guide sockets.

T2-OBS-0880: The actual keying positions of the Plug-In Modules will depend on the orientation of the keying pins of the Backplane slot the baseboard is interfacing with.

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T2-REC-0045: With higher shock and vibration environments, Payload and Switch Modules **should** use the RT 2-R rugged connectors.

T2-REC-0046: Alignment pin keying information for Plug-In Modules **should** be documented.

T2-RUL-3720: Plug-In Modules **shall** prohibit features that prevent installation in a HOST Enclosure.

T2-RUL-3730: No additional components **shall** be required to install a Plug-In Module in a HOST Enclosure other than those typically used for ANSI/VITA compliant OpenVPX modules.

5.3.2.2.2.1 **6U Interfaces**

T2-RUL-3690: 6U Power Supply Modules **shall** follow the rules defined in ANSI/VITA 62.0, section 4.3.2 6U Slot Keying and in section 6.3 Alignment and Keying.

T2-RUL-3700: 6U Payload and Switch Modules **shall** use connectors defined in ANSI/VITA 46.0, Table 6-1, or the rugged equivalent RT 2-R, unless following SECTION 5.1.1.1.2.4 or SECTION 5.1.1.3.2.3.

T2-PER-0205: 6U Payload and Switch Modules **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.2.4 and SECTION 5.1.1.3.2.3.

5.3.2.2.2.2 **3U Interfaces**

T2-RUL-3701: 3U Power Supply Modules **shall** follow the rules defined in ANSI/VITA 62.0, section 4.3.1 3U Slot Keying and in section 5.3 Alignment and Keying.

T2-RUL-3702: 3U Payload and Switch Modules **shall** use connectors defined in ANSI/VITA 46.0, Table 5-1, or the rugged equivalent RT 2-R, unless following SECTION 5.1.1.1.3.4 or SECTION 5.1.1.3.3.3.

T2-PER-0206: 3U Payload and Switch Modules **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.3.4 and SECTION 5.1.1.3.3.3.

5.3.2.2.3 **Environmental Requirements**

T2-RUL-3740: Plug-In Modules **shall** perform to a minimum Environmental Class ECC4 as defined in ANSI/VITA 47.0.

T2-RUL-3750: Plug-In Module vibration response for each axis **shall** be provided for a 5-2000 Hz sine sweep at 1G amplitude with a rate ranging from 1 to 5 octaves/minute, measured at the card center of mass.

T2-RUL-3751: Plug-In Module Vibration response for each axis **shall** be monitored and controlled at the card guide interface with the HOST Module for these Tests.

T2-OBS-0890: A test setup required to perform vibration testing is available in the component registry.

T2-RUL-3770: Modules that perform in environments not included in the ANSI/VITA 47.0 standard **shall** provide information on acceptable environmental conditions.

T2-RUL-3780: Conformal coating for Modules **shall** be applied per IPC-J-001F.

T2-RUL-3790: Materials used for conformal coating **shall** conform to IPC-CC-830B and be included in QPDSIS-46058.

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5.3.2.2.4 **Liquid-Cooled Modules**

To be developed in a future revision of this standard.

5.3.2.3 **HOST Transmission Components**

HOST Transmission Components facilitate physical connectivity of power and communications signals between HOST Modules. The standard transmission component for OpenVPX is a Backplane that interfaces with standard Plug-In Modules. This standard defines the required form factor, interfaces, environmental requirements, and documentation requirements for the HOST OpenVPX Backplane.

5.3.2.3.1 **Form Factor**

The form factor for standard HOST OpenVPX Backplane is defined in ANSI/VITA 65.0, section 4. ANSI/VITA 65.0 essentially passes these requirements through from ANSI/VITA 46, which refer to standard form factors defined in IEEE 1101.1 and IEEE 1101.2. FIGURE 5-17 shows the required 6U slot form factor derived from these standards and FIGURE 5-18 shows the required 3U slot form factor.

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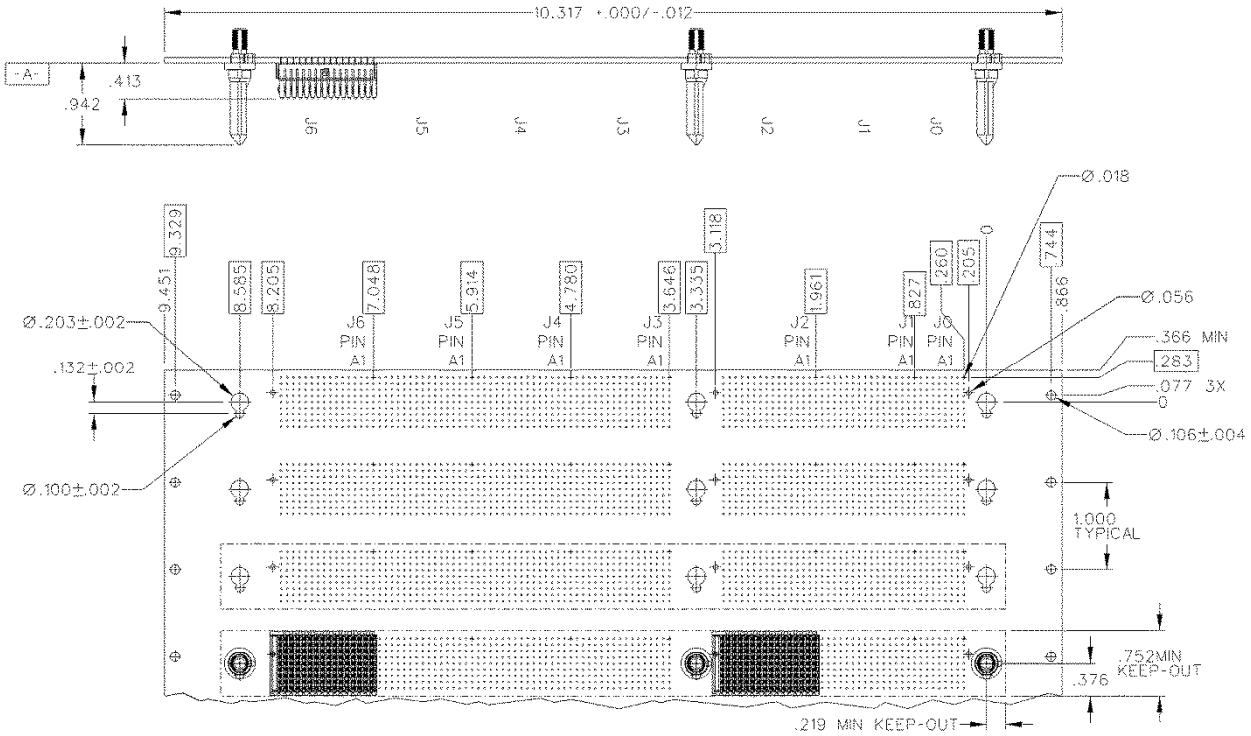

Figure 5-17 – 6U OpenVPX Backplane Form Factor

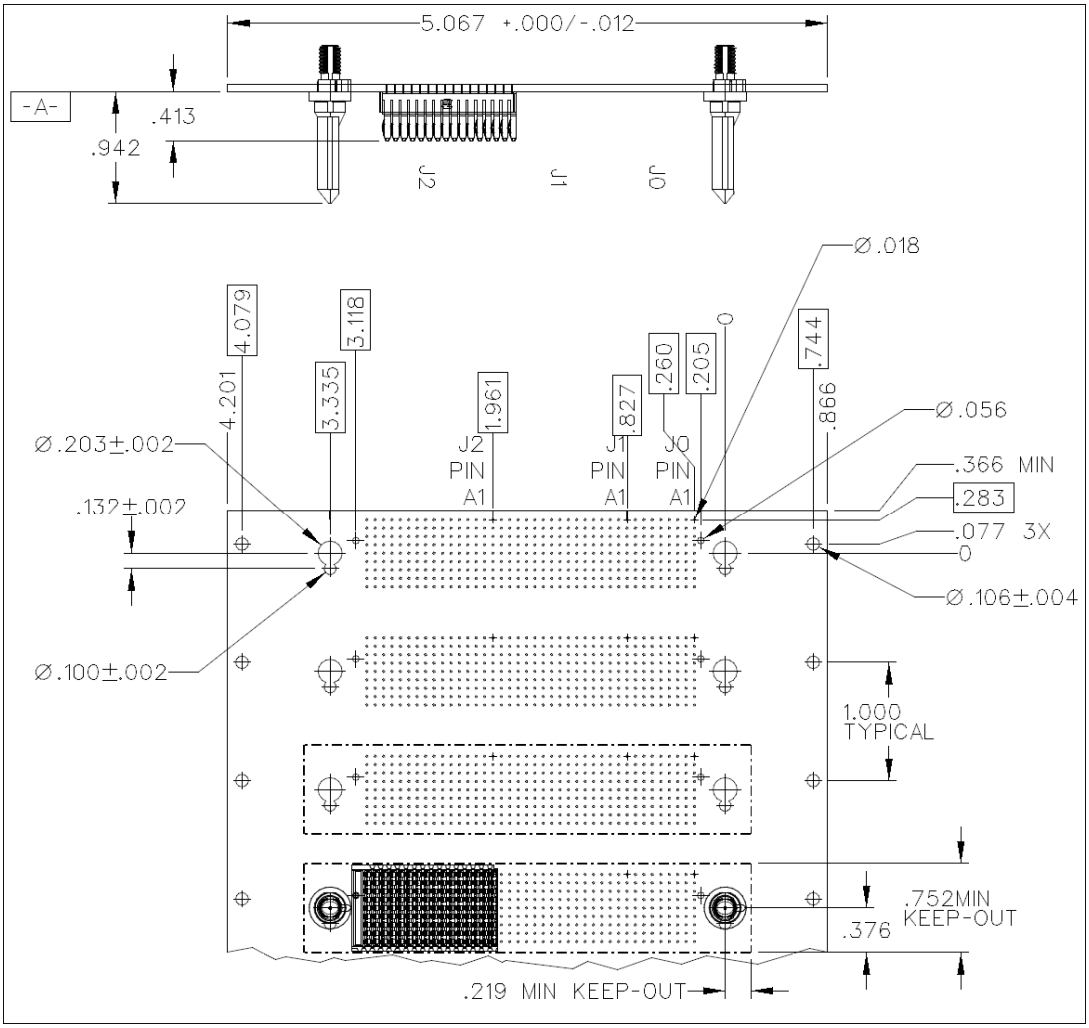

Figure 5-18 – 3U OpenVPX Backplane Form Factor

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T2-OBS-0900: FIGURE 5-17 and FIGURE 5-18 are derived from the requirements in ANSI/VITA 65. For clarification, refer to ANSI/VITA 65.0 and its related documents.

T2-RUL-3800: Backplanes **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
3. Requirements of ANSI/VITA 65.0 for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

5.3.2.3.2 Interfaces

T2-RUL-3810: Backplanes **shall** conform to the interface requirements defined in ANSI/VITA 65.0.

T2-RUL-2480: Backplanes **shall** have a 1 inch slot pitch.

T2-RUL-3820: Backplane Payload, Switch, Power Supply, and Energy Storage Slots **shall** use alignment and keying pins called out in ANSI/VITA 46.0, Observation 7-22.

T2-RUL-3890: Power supply module slots **shall** use connectors defined in ANSI/VITA 62.0, Table F-1.

T2-REC-0047: Alignment pin keying information for Backplanes **should** be documented.

T2-RUL-3910: Transmission components **shall** prohibit features that prevent installation of a HOST Module.

T2-RUL-3920: No additional non-COTS components **shall** be required to install a HOST Module.

5.3.2.3.3 6U Interface Requirements

T2-RUL-3830: Backplane 6U Power Supply Module Slots **shall** be keyed in accordance to ANSI/VITA 62.0, section 4.3.2 6U Slot Keying.

T2-RUL-3840: Key position 1 for Backplane 6U Payload slots **shall** be set to 315 degrees.

T2-RUL-3850: Key position 1 for Backplane 6U Switch slots **shall** be set to 315 degrees.

T2-RUL-3860: If Backplane keys are for slot 1, key positions 2 and 3 for Backplane 6U Payload slots **shall** be set to angle 270.

T2-RUL-3870: If Backplane keys are for slot 1, key positions 2 and 3 for Backplane 6U Switch slots **shall** be set to angle 270.

T2-RUL-3861: Key positions 2 and 3 for Backplane 6U Payload and Switch slots **shall** change angles after slot 1 with position 2 acting as the "least significant bit" and position 3 acting as the "most significant bit", where position 2 goes through the angles in the following order: 270, 315, 0, 45, 90 before position 3 goes from 270 to 315. This continues for as many slots as there are in the Backplane.

T2-OBS-0078: The numbering for the key positions is called out in ANSI/VITA 46.0, Rule 4-12.

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T2-OBS-0910: The keying position rules come from recommendation 7-17 of ANSI/VITA 46.0.

T2-RUL-3880: 6U Payload and Switch slots **shall** use connectors defined in ANSI/VITA 46.0, Table 6-1, or the rugged equivalent RT 2-R, unless the slot is utilized for a Module following SECTION 5.1.1.1.2.4 or SECTION 5.1.1.3.2.3.

T2-PER-3881: 6U Payload and Switch slots **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.2.4 and SECTION 5.1.1.3.2.3.

5.3.2.3.4 **3U Interface Requirements**

T2-RUL-3881: Backplane 3U Power Supply Module Slots **shall** be keyed in accordance to ANSI/VITA 62.0, section 4.3.1 3U Slot Keying.

T2-RUL-3882: If Backplane keys are for slot 1, key positions 1 and 2 for Backplane 3U Payload slots **shall** be set to angle 270.

T2-RUL-3883: If Backplane keys are for slot 1, key positions 1 and 2 for Backplane 3U Switch slots **shall** be set to angle 270.

T2-RUL-3884: Key positions 1 and 2 for Backplane 3U Payload and Switch slots **shall** change angles after slot 1 with position 1 acting as the "least significant bit" and position 2 acting as the "most significant bit", where position 1 goes through the angles in the following order: 270, 315, 0, 45, 90 before position 2 goes from 270 to 315. This continues for as many slots as there are in the Backplane.

T2-OBS-0911: The numbering for the key positions is called out in ANSI/VITA 46.0, Rule 4-12.

T2-OBS-0912: The keying position rules come from recommendation 7-18 of ANSI/VITA 46.0.

T2-RUL-3885: 3U Payload and Switch slots **shall** use connectors defined in ANSI/VITA 46.0, Table 5-1, or the rugged equivalent RT 2-R, unless the slot is utilized for a Module following SECTION 5.1.1.1.3.4 or SECTION 5.1.1.3.3.3.

T2-PER-3882: 3U Payload and Switch slots **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.3.4 and SECTION 5.1.1.3.3.3.

5.3.2.3.5 **Environmental Requirements**

T2-RUL-3930: Transmission Components **shall** perform to a minimum Environmental Class ECC4 as defined in ANSI/VITA 47.0.

T2-RUL-3940: Conformal coating for Backplanes **shall** be applied per IPC-J-001F.

T2-RUL-3950: Materials used for conformal coating **shall** conform to IPC-CC-830B and be included in QPDSIS-46058.

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6 Glossary

Term	Definition
Analysis	Analysis is an element of verification that uses generally accepted technical methods including mathematical models or simulations, algorithms, charts, graphs, circuit diagrams, data, or other scientific principles and procedures to determine conformance with specified requirements. "Generally accepted", in this context, means in accordance with common design engineering practices.
Backplane Profile	A physical definition of a backplane implementation that includes details such as the number and type of slots that are implemented and the topologies used to interconnect them. Ultimately a Backplane Profile is a description of Channels and Buses that interconnect slots and other physical entities in a backplane.
Chassis Domain Inventory Information Record	Chassis Domain Inventory Information Records contain the hardware-specific information necessary to uniquely identify and verify the configuration of the HOST Chassis it represents. The information typically contained in Inventory Information Records includes serial number, part number, model, inventory number ("asset tag"), and the version numbers for any manufacturer-installed software or firmware.
Chassis Management Transmission Interface	The CMTI provides connectivity between Chassis Management entities (Managers, Participants, and Remote Participants). The CMTI provides chassis management and utility capabilities such as health monitoring, status reporting, maintenance, system reset, system power-up/power-down management, and system recovery. The CMTI can share a physical transmission medium with other transmission interfaces but it remains logically distinct based upon the type of data that it carries.
Command	A Command is communication from a Manager indicating to one or more Participants that some action will be performed.
Commercial-Off-the-Shelf	A commercial item sold in substantial quantities in the commercial marketplace and offered to the government under a contract or subcontract, without modification, in the same form in which it was sold in the marketplace.
Data Storage Resources	DSRs perform mass storage functions. Data storage can be implemented as a large, monolithic storage resource or as a collection of distributed resources. Modules that implement data storage must support the SCTI since that is the exclusive communications interface between data storage and other resources.

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Term	Definition
Demonstration	Demonstration is an element of verification that involves the qualitative exhibition of functional performance. While test equipment might be required as part of the Demonstration setup, measurements are typically not required. Demonstration might also be used when requirements or specifications are given in statistical terms (e.g., average power consumption, mean time to repair, etc.).
External I/O Transmission Interface	The EIOTI provides a method for connecting Platform I/O and power signals to the System I/O and Power Distribution Interfaces where they can then be accessed by I/O processing and PSRs. The EIOTI will typically take the form of front and/or rear panel chassis I/O connection systems that utilize any combination of cabling, rigid printed wiring board (PWB), or flex PWB.
Field Replaceable Unit	An electronic hardware component that can be removed and replaced without sending the product to a repair facility. Throughout this Tier 2 HOST Standard, "FRU" should be interpreted as "HOST Module."
General Processing Resources	GPRs perform generic data processing functions. General Processing can be implemented as a large, monolithic processing block or as a collection of small, distributed processing units. The distinction between general and I/O processing is established logically and not physically, in that GPRs do not directly affect changes in external I/O. IOPRs directly affect changes in external I/O. Modules that implement general processing must support the SCTI since that is the exclusive communications interface between general processing and other resources.
HOST Backplane	A physical circuit card assembly that accepts HOST Plug-In Modules and provides access to the Transmission Interfaces.
HOST Chassis	A HOST Chassis is the aggregate collection of HOST Modules governed by a single Manager.
HOST Component	A physical device or software product that is defined, in whole or part, by requirements in the HOST Standards.
HOST Enclosure	A physical chassis that holds together all of the HOST Components in a Target System implementation.
HOST External Interface	Physical connection between the HOST Transmission Components and the external system.
HOST Management	An autonomous subsystem that provides application independent hardware management and monitoring capabilities for the module, chassis, and system domains.

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Term	Definition
HOST Mezzanine Module	A HOST Component that contains functionality as defined by the HOST Resources and a physical form factor that conforms to the requirements of this HOST Tier 2 OpenVPX Standard for mezzanines.
HOST Module	A HOST Component that contains logical and physical functionality as defined by the HOST Resources, utilizes one or more HOST Transmission Interfaces, and is visible to the HOST Chassis Management Architecture. HOST Modules are managed by Participant functionality. Participants exist at the Module Domain level to each oversee a single HOST Module's configuration, BIT, fault logging, startup, etc. Examples of Tier 2 HOST Module implementations can include: printed wiring Plug-In Modules, mezzanine modules, power supply modules, etc.
HOST Plug-In Module	A HOST Component that contains functionality as defined by the HOST Resources and plugs directly into a backplane.
Image Processing Resources	IPRs perform dedicated image and graphics processing functions. The distinction between image and general processing is established logically and not physically, in that IPRs are specifically designated to directly manipulate image, video, or graphics data buffers while GPRs are not. IPRs can also directly affect changes in external I/O if those I/O are analog or digital video signals through system I/O. Modules that implement image processing must support the SCTI since that is the exclusive communications interface between image processing and other resources. Modules that implement image processing can also support the SIOTI since that is the exclusive transmission interface for analog and digital video signals between image processing and external I/O.
Inspection	Inspection is an element of verification that involves an examination of the item/system or drawing form. Drawing forms are any controlled document that defines the product configuration for design, assembly, or Test. Inspection may include gauging or measurement.
Intelligent Platform Management Bus	Name for the architecture, protocol, and implementation of a special bus that interconnects the baseboard and chassis electronics and provides a communications media for system platform management information.
I/O Processing Resources	IOPRs perform I/O processing functions on external I/O that pass through the EIOTI. The distinction between I/O and general processing is established logically and not physically, in that IOPRs directly affect changes in external I/O and GPRs do not. Modules that implement I/O processing must support the SCTI since that is the exclusive communications interface between I/O processing and other resources. Modules that implement I/O processing must also support the SIOTI since that is the exclusive transmission interface between I/O processing external I/O.

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Term	Definition
Manager	The Manager is a software or firmware entity that manages Participants within the Chassis Domain. The Manager communicates with Participants via the HOST CMTI utilizing MPP.
Manager/Participant Protocol	An open, standardized, non-proprietary means of data exchange that ensures interoperability between HOST Modules and guarantees support for a fundamental set of functionality.
Module Domain Event Log	Module Domain Event Logs are maintained for the storage of hardware events, faults, and anomalies at the module level for the HOST Module the Participant is representing in the chassis.
Module Domain Inventory Information Record	A Module Domain Inventory Information Record contains the hardware-specific information necessary to uniquely identify and verify the configuration of the HOST Module it represents. The information typically contained in Inventory Information Records includes serial number, part number, model, inventory number (“asset tag”), and the version numbers for any manufacturer-installed software or firmware.
Module Profile	A physical mapping of ports onto a given Module's backplane Connectors and protocol mapping(s), as appropriate, to the assigned Port(s). This definition provides a first-order check of operating compatibility between Modules and slots as well as between multiple Modules in a Chassis. Module Profiles achieve the physical mapping of ports to backplane connectors by specifying a Slot Profile. Multiple Module Profiles can specify the same Slot Profile.
Participant	A Participant is a software or firmware entity that resides on a HOST Module and manages the Module Domain functional resources on that HOST Module. Participants communicate with Manager via the CMTI utilizing MPP.
Platform	A vehicle or weapons system on which a HOST based system will be installed (e.g. an aircraft).
Power Supply Resources	PSRs transform Target System power into chassis power that is supplied to HOST Modules via the system power distribution segment. Modules that implement PSRs must support the Power Distribution Interface since that is the exclusive power distribution interface for HOST Modules.
Proxied HOST Module	A Proxied HOST Module is a hardware module represented by a Remote Participant that incorporates a proxy implementing software, firmware, and/or hardware translation.
Remote Participant	A Remote Participant is a software or firmware entity that resides on a HOST Module and represents a Proxied HOST Module that is not capable of communicating in a manner consistent with MPP.

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Term	Definition
Response	A Response is communication from a Participant containing information in response to a MPP Command.
Slot Profile	A physical mapping of ports onto a given slot's backplane connectors. These definitions are often made in terms of Pipes. Slot Profiles also give the mapping of Ports onto Plug-In Module's backplane connectors. Unlike Module Profiles, a Slot Profile never specifies protocols for any of the defined Ports.
Standby Manager	A software or firmware entity that is capable of assuming all Manager duties in the event of Manager loss or critical failure.
System Communications Transmission Interface	The SCTI carries general communications data between resources. General communications data consists of resource coordination and data messages required for general computing performance. The SCTI does not carry Platform I/O signals between resources. The SCTI can share a physical transmission medium with other Transmission Interfaces but it remains logically distinct based upon the type of data that it carries. The SCTI could be implemented as an address mapped parallel bus, a packet-switched network, or any number of other communications methods.
System I/O Transmission Interface	The SIOTI connects I/O signals between the EIOTI and I/O resources. The SIOTI does not carry general communications data between resources (i.e. data allocated to the SCTI).
System Power Distribution Interface	The SPDI distributes power from the Power Supply modules within the PSR to all modules requiring power. The power specifications and transmission methods are specific to a Tier 2 core technology standard.
Test	Test is an element of verification designed to provide data on functional features, performance, or equipment operation under fully controlled and traceable conditions. Test generally use special instrumentation or test equipment to obtain accurate the quantitative data for Analysis. The data is used to evaluate quantitative characteristics. Testing implicitly requires Analysis of the resulting test data.
Target System	A HOST based aggregation of components/modules intended to carry out a defined function on a Platform (e.g. a mission computer).

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7 Acronyms

CMTI – Chassis Management Transmission Interface

COTS – Commercial-Off-the-Shelf

CVAM – Conformance Verification and Applicability Matrix

CVM – Conformance Verification Matrix

DSR – Data Storage Resource

EIOTI – External I/O Transmission Interface

FRU – Field Replaceable Unit

GPR – General Processing Resource

HOST – Hardware Open System Technologies

HOST-MGMT – Hardware Open System Technologies - Management

HOVM – HOST OpenVPX Verification Methods

IOPR – I/O Processing Resource

IPR – Image Processing Resource

IPMB – Intelligent Platform Management Bus

IPMC – Intelligent Platform Management Controller

IPMI – Intelligent Platform Management Interface

MPP – Manager/Participant Protocol

PSR – Power Supply Resource

SCTI – System Communications Transmission Interface

SDR – Sensor Data Record

SIOTI – System I/O Transmission Interface

SPDI – System Power Distribution Interface

VA – Verification Authority

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