HARDWARE OPEN SYSTEMS TECHNOLOGIES

Hardware Open Systems Technologies OpenVPX Core Technology Tier 2 Standard

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1 Overview

1.1 Objective

The Tier 2 *Hardware Open System Technologies* (HOST) OpenVPX Core Technology Standard applies OpenVPX embedded computing technologies to the HOST Tier 1 Standard architecture. This document introduces the application of OpenVPX as a Core Technology Standard, defines the conventions and conformance standards used in the document, and defines specific requirements of this Core Technology Standard.

1.2 HOST– OpenVPX Core Technology

The HOST OpenVPX Core Technology Standard defines technical requirements applying OpenVPX embedded computing technologies to the HOST Architecture. HOST Tier 2 standards are *Platform* agnostic, so this standard does not incorporate specific requirements of *Target Systems*. The goals of this HOST Core Technology Standard are to:

- Apply OpenVPX embedded computing technologies and leverage ANSI/VITA 46.11 for hardware system management to define Target System agnostic requirements
- Facilitate OpenVPX computing hardware interoperability and reuse
- Facilitate the extensive use of OpenVPX *Commercial-Off-the-Shelf* (COTS) components
- Enable the derivation of HOST Tier 3 component specifications from the combination of the HOST Tier 1 Standard, HOST Tier 2 Standard, and Target System requirements

Throughout the document, the standard is referred to interchangeably by the following terms: “HOST Tier 2 Standard,” “Tier 2 HOST Standard,” and “Tier 2 Core Technology Standard.”

1.3 Referenced Documents

ANSI/VITA 42.0-2008 (R2014), Switched Mezzanine Card (XMC)

ANSI/VITA 42.3-2006 (R2014), XMC PCI Express Protocol Layer Standard

ANSI/VITA 46.0-2013 (R2013), VPX Base Standard

ANSI/VITA 46.6-2013, Gigabit Ethernet Control Plane on VPX

ANSI/VITA 46.9-2017, PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard

ANSI/VITA 46.11-2015, System Management on VPX

ANSI/VITA 47-2005, Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard

ANSI/VITA 48.2-2010, Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to ANSI/VITA VPX

ANSI/VITA 62.0-2012, Modular Power Supply Standard

ANSI/VITA 65.0-2017, OpenVPX

ANSI/VITA 65.1-2017, OpenVPX System Standard – Profile Tables

ANSI/VITA 66.0-2016, Optical Interconnect on VPX – Base Standard

ANSI/VITA 67.0-2012, Coaxial Interconnect on VPX – Base Standard

ANSI/VITA 67.3-2016, Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane

IEEE 802.3-2012 (December 28, 2012), IEEE Standard for Ethernet

IEEE 1101.2-1992 (January 31, 20008), IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards

IEEE 1386.1-2001 (June 14, 2001), IEEE Standard Physical and Environmental Layers for PCI Mezzanine

Intelligent Platform Management Interface (IPMI) Specification Version 2.0, Revision 1.1, dated 01 October 2013

IPC J-STD-001F (July 2014), Requirements for Soldered Electrical and Electronic Assemblies

IPC-CC-830B with Amendment 1 (October 2008), Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPMI Platform Management FRU Information Storage Definition Version 1.0, Revision 1.2, dated 28 February 2013

QPDSIS-46058 Insulating Compound, Electrical, dated 22 June 2017

2 Implementation

This Tier 2 HOST Standard governs the implementation of HOST conformant *system*s utilizing the ANSI/VITA 65.0 OpenVPX System Specification and related embedded computing standards. More specifically, this Tier 2 Architecture defines the implementation of the following HOST Architecture elements with OpenVPX as the core technology for Hardware. ANSI/VITA 46.11 and IPMI standards are leveraged for hardware management.

2.1 Hardware System Management

Hardware System Management Architecture establishes an autonomous subsystem that provides application independent hardware management and monitoring capabilities for the module, chassis, and system domains. Hardware System Management implements Sensor Management, System/Module Inventory and Configuration, SW/FW Management, Field Replaceable Unit (FRU) Recovery, and Diagnostic Management capabilities. This Tier 2 HOST Standard extends ANSI/VITA 46.11 and IPMI standards to define the required data exchanges and Hardware System Management messages.

2.2 Hardware Implementation

This Tier 2 HOST Standard standardizes hardware components and their interfaces to facilitate interoperability between the components residing in a chassis.

2.2.1 HOST Components

HOST Components are divided into four main categories: Modules, External Interfaces, Transmission Interfaces, and the Enclosure.

2.2.1.1 HOST Modules

HOST Modules are implemented as a *Plug-In* or as *HOST Mezzanine Modules*.

HOST Plug-In Modules are implemented using ANSI/VITA 65.0/ANSI/VITA 48.2 Conduction-cooled Payload and Switch Modules, and ANSI/VITA 62.0 Power Supplies.

HOST Mezzanine Modules are implemented using ANSI/VITA 42.0/42.3 *Switched Mezzanine Cards* (XMC) Standard and IEEE 1385 PCI Mezzanine Cards (PMC).

2.2.1.2 HOST External Interface

HOST External interfaces provide the physical connection, transfer signals and power between the HOST Transmission Components and the external system.

2.2.1.3 Transmission Interface

Transmission Interfaces are responsible for the logical and physical connectivity within the system. For this Tier 2 core technology, Transmission Interfaces are implemented utilizing backplanes composed of HOST-specific and ANSI/VITA 65.0 design elements.

2.2.1.4 HOST Enclosure

The *HOST Enclosure* is implemented utilizing ANSI/VITA 48.2 and ARINC 404 1-ATR Enclosure design elements.

2.3 Resource Implementation

Although this Tier 2 HOST Standard is based primarily upon the use of OpenVPX as the core technology, it will further define requirements for making OpenVPX components HOST conformant. Therefore, a component that is OpenVPX conformant is not necessarily HOST conformant.

FIGURE 2.3-1 shows an example of how the resources could be implemented on different HOST Modules.

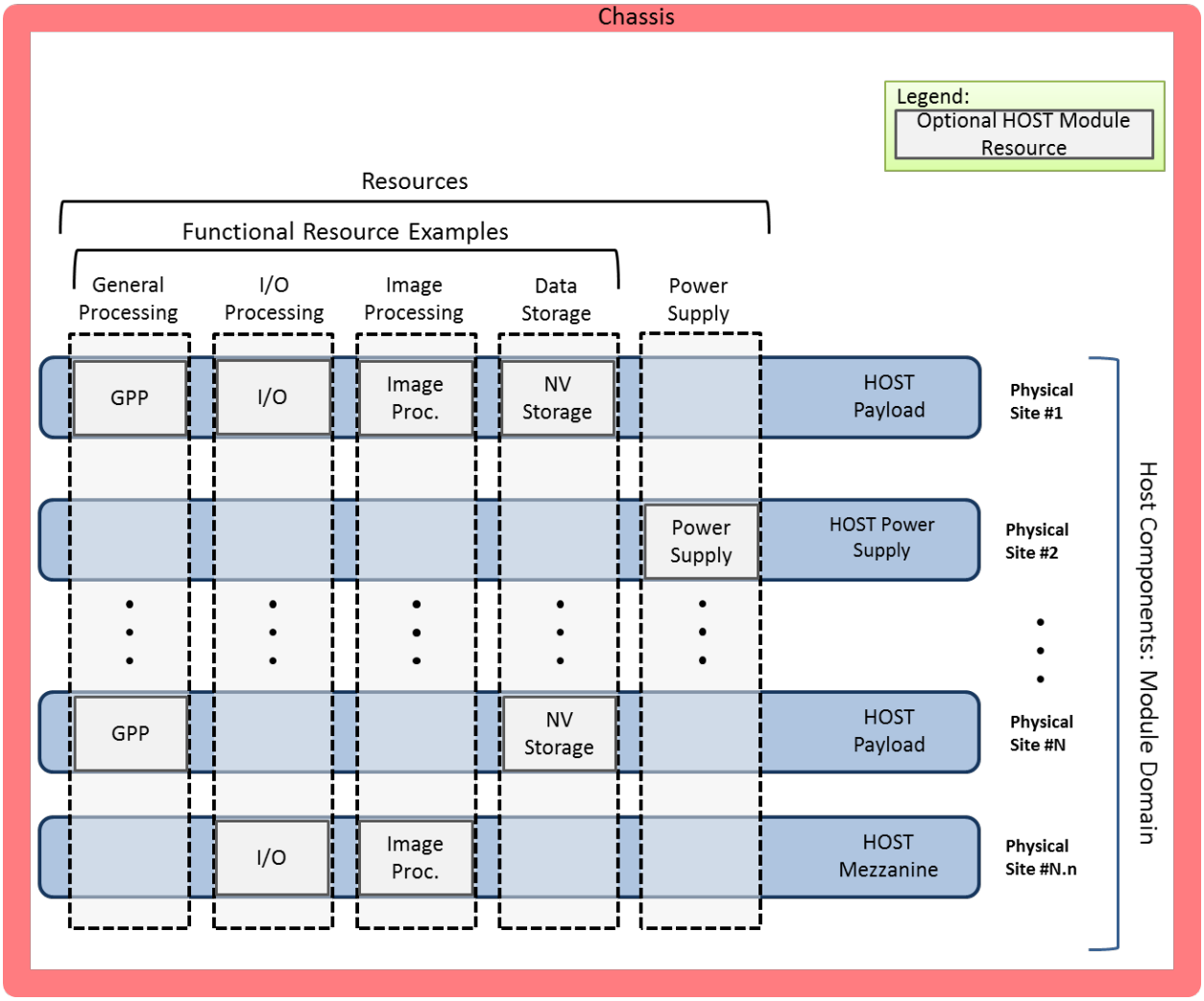

Figure 2.3-1 – Resource Implementation Example

In FIGURE 2.3-1 the HOST Payload Module is based on an ANSI/VITA 65.0 Plug-In Module, the HOST Mezzanine could be either a PMC or XMC module, and the HOST Power Supply is based on an ANSI/VITA 62.0 Power Supply Plug-In Module. (Note: Terminology in this standard follows the ANSI/VITA standard where a mezzanine is interchangeably called a card or module.)

3 Guidelines

3.1 Typography

The following typographical conventions are used throughout this document:

- *Italics* – Indicates a term defined in the glossary or for emphasis (occurs on first instance).
- **Bold** – Indicates keywords and their terms (ex: “shall”, “should”, “may”) as defined in Section 3.2.
- SMALL CAPS - Cross-reference to another section, figure, or table in this document.

3.2 Keywords

To avoid confusion and to make clear what the requirements for conformance are, many of the paragraphs in this standard are labeled with keywords that indicate the type of information they contain. These keywords are listed below:

• Rule
• Recommendation
• Permission
• Observation

Any text not labeled with one of these keywords is to be interpreted as descriptive in nature. These will be written in either a descriptive or a narrative style.

Keywords are reserved for specific use as defined in subsequent sections. References to a section or paragraph from an external source that are included in a Keyword statement will also contain all lower level sections and paragraphs.

3.2.1 Rule

Compliance with rules is mandatory. Rules always include the term “shall.” Rules are expressed in some combination of text, figures, tables, or drawings. All rules will be followed to ensure compatibility across interfaces.

3.2.2 Recommendation

Compliance with Recommendations is optional. Recommendations always include the term “should.” Recommendations are used to convey implementation advice based on the community’s collective knowledge base. Recommendations found in this standard are provided to designers to reduce their learning curve.

3.2.3 Permission

Compliance with Permissions is optional. Permissions always include the term “may.” In some cases, a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable.

3.2.4 Observation

Observations do not offer any specific advice. They are provided to enhance comprehension and usually follow naturally from what has just been discussed. They spell out the implications of certain rules and

bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands the spirit of the rule.

4 HOST Conformance

Defining conformance and creating a method for verifying and certifying HOST products is vital to establishing an effective standard. Certification provides formal recognition of conformance to a HOST standard or specification. Without the associated conformance criteria and processes, there is no assurance that a supplier has developed or implemented products or solutions according to the approved HOST Technical Standards and Specifications. Verification provides evidence of conformance to a HOST Technical Standard or Specification, which allows:

- Buyers to specify and successfully procure hardware from vendors who provide solutions that conform to the HOST Specifications and Standards.
- System Integrators to make and substantiate clear claims of conformance to HOST Specifications and/or Standards.
- Hardware component suppliers to make and substantiate clear claims of conformance to HOST Specifications.

The government will establish conformance criteria and define an associated Conformance Program for the HOST Tier 3 Specifications and HOST Components.

The conformance assessment is intended to certify compliance with HOST requirements and is not intended to ensure a component or system will function as intended in its final application. Conformance assessment is not meant to assist with or replace developmental or operational test.

4.1 HOST Conformance Program

The HOST Conformance Program will have two primary functions:

1) Verification that a newly developed or revised Tier 3 Specification complies with the requirements of the applicable HOST Tier 2 Standard.
2) Verification that a hardware component complies with the requirements of the applicable HOST Tier 3 Specification.

4.1.1 HOST Conformance Program Terminology

HOST Conformance is defined as 100 percent compliant with all HOST requirements.

HOST Verification is the act of determining the conformance of a HOST product to the applicable HOST Technical Standard or Specification requirements. The applicable Tier 2 Standards and Tier 3 Specification will have associated matrices that recommend or specify a verification method for each rule. Verification will be carried out by the agency responsible for developing the HOST product being verified. Results and artifacts of the verification will be submitted to a Verification Authority (VA). The VA will review the verification results and artifacts to make a determination on whether the verification process was sufficiently correct and complete to show conformance to the next higher level specification or standard.

Publication is the process of entering a HOST Specification into a registry. Specifications residing in the registry will be available to outside Government agencies and commercial companies. Distribution of the published document will be controlled by the distribution statement on the cover page.

HOST Registration is the process of listing Certified HOST Tier 3 Specifications and HOST Components in a public listing known as the HOST Registry.

4.1.2 HOST OpenVPX Verification Methods Document

Detailed verification method information required for Tier 3 Specifications that conform to the requirements of this document are detailed in a companion document to this standard titled: *HOST OpenVPX Verification Methods* (HOVM).

The HOVM contains a *Conformance Verification and Applicability Matrix* (CVAM). The CVAM will include entries for all HOST Tier 2 requirements and identify, at a minimum, the following details for each Tier 2 rule: requirement ID, applicability to the specific types of components identified in the Tier 2 Standard, recommended verification method for the requirement, and additional information as necessary. The HOVM also defines the types of documentation that are required for verification of a Tier 3 Specification.

4.1.3 HOST Tier 3 Specification Conformance

Tier 3 Specifications will be verified to show conformance to this Tier 2 Standard. The agency authoring the Tier 3 Specification will perform and document a requirements trace to show that all applicable rules of this document have been flowed down to the Tier 3 Specification. In addition, a check will be made to verify that the Tier 3 Specification's *Requirements Verification Matrix* (RVM) covers all of the requirements identified in the Tier 3 Specification. The Tier 3 RVM will be checked to verify that it lists the appropriate verification methodology for each requirement per the CVAM contained in the HOVM. The submitting agency will provide the results of their verification efforts and supporting documentation to be reviewed by the VA. Upon successful completion of the HOST Tier 3 conformance process, the Tier 3 Specification will be published.

4.1.4 HOST Component Conformance

Components will be verified to show conformance to the applicable HOST Tier 3 Specification. Verification methods for component requirements will be identified in an RVM included in the Tier 3 Specification. The submitting agency will perform verification of the developed product to show conformance to the Tier 3 Specification. The submitting agency will provide the results of their verification efforts and supporting documentation to be reviewed by the VA. Upon successful completion of the HOST conformance process and review by the VA, the component data will be entered into the HOST Registry.

T2-RUL-0005: HOST Modules **shall** conform to one or more HOST Tier 3 Specifications.

T2-PER-0001: Non-Module HOST Components **may** conform to one or more HOST Tier 3 Specifications.

T2-RUL-0016: Level A Conformant Modules **shall** implement all applicable rules within this standard.

T2-RUL-0017: Level B Conformant Modules **shall** implement all rules except SECTION 5.3 Hardware System Management Rules.

4.1.5 Requirements Verification Matrix

The Tier 3 Specification will include an RVM. The purpose of the RVM is to identify the required verification method for each Tier 3 Specification requirement. The RVM will identify whether or not each Tier 3 requirement traces to a HOST Tier 2 Standard requirement. In addition, the RVM will include the required verification method, an indication on whether each Tier 3 requirement was derived from

this HOST Tier 2 Standard, the product specification, or both. For clarity, the RVM shall include entries for Tier 2 rules that are not applicable to the HOST component. These rules will be identified as not applicable.

T2-RUL-0001: A HOST Tier 3 Specification conforming to this standard **shall** include an RVM that includes one or more entries for each rule of this standard.

T2-RUL-0002: For each Tier 3 requirement, the Tier 3 RVM **shall** indicate whether the requirement was derived from a HOST Tier 2 rule, the product specification or both.

T2-RUL-0018: For each Tier 3 requirement that traces to one or more HOST Tier 2 rules, the Tier 3 RVM **shall** identify which Tier 2 rules trace to that Tier 3 requirement.

T2-RUL-0019: For each Tier 3 requirement, the Tier 3 RVM **shall** specify the required verification method.

T2-RUL-0004: For each Tier 2 rule applicable to the type of component specified in Tier 3, the Tier 3 Specification **shall** identify the required artifacts and any additional information required for verification.

T2-RUL-0021: For each Tier 2 rule that does not apply to the HOST component type specified by the Tier 3 as specified by the CVAM, the RVM **shall** contain an entry which identifies that Tier 2 rule as not applicable.

4.1.6 Verification Methods

HOST Component requirements will be based on one of the following conformance methods: *Inspection*, *Analysis*, *Demonstration*, or *Test*.

5 Tier 2 Standard Requirements

5.1 HOST Module Requirements

This HOST Tier 2 Core Technology Standard implements HOST Modules as 6U and 3U OpenVPX Plug-In Modules, ANSI/VITA 62.0 Power Supply Plug-In Modules, and PMC/XMC Mezzanine Modules. HOST Plug-In Modules consist of HOST Payload Modules, HOST Switch Modules and HOST *Power Supply Modules* (PSM) that connect (plug-in) directly to the *HOST Backplane* component. HOST Payload Modules are used to implement the *Functional Resources* (FR) and/or act as carriers of HOST Mezzanine Modules. HOST Switch Modules provide *System Communications Transmission Interface* (SCTI) interconnection between HOST Payload Modules. HOST Power Supply Modules transform Platform power into system power for use by HOST Payload and Switch modules.

The hierarchy of rules for the various HOST Module types is shown in FIGURE 5.1-1.

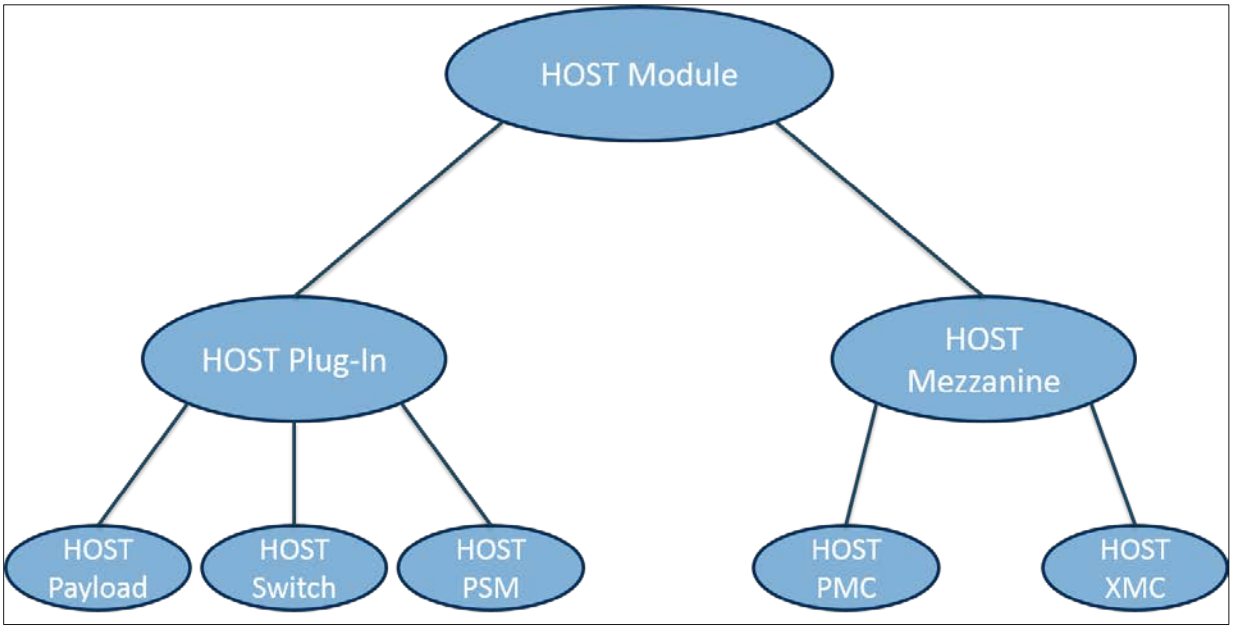

Figure 5.1-1 – HOST Module Rules Hierarchy

The module hierarchy clarifies which rules each module type must follow. For example, a HOST Switch must follow any rules levied on HOST Switches, HOST Plug-Ins, and HOST Modules; but a HOST Switch does not have to follow rules levied on HOST Payloads, HOST PSMs, or HOST Mezzanines Modules.

T2-RUL-0010: For this Tier 2 Core Technology Standard a HOST Module **shall** be defined as a Payload Module, Switch Module, Power Supply Module, PMC Mezzanine Module, or a XMC Mezzanine Module.

T2-RUL-0011: Payload, Switch, and Power Supply Modules **shall** conform to the requirements of HOST Plug-In Modules.

T2-RUL-0012: PMC and XMC Modules **shall** conform to the requirements of HOST Mezzanine Modules.

T2-RUL-0020: A HOST Module **shall** conform to interface requirements of the *Chassis Management Transmission Interface* (CMTI) per SECTION 5.4.1.5.

T2-PER-0010: A HOST Module **may** utilize the *System I/O Transmission Interface* (SIOTI) per SECTION 5.4.1.3.

T2-RUL-0030: A HOST Module **shall** conform to the interface requirements of the *System Power Distribution Interface* (SPDI) per SECTION 5.4.1.6.

T2-RUL-0052: HOST Modules **shall** leave signals HOST defines as reserved unconnected.

T2-PER-0012: A HOST Module **may** have only a subset of the SPDI voltages defined within the OpenVPX Utility Plane as an input.

T2-RUL-0031: If a HOST Module uses only a subset of the SPDI voltages defined within the OpenVPX Utility Plane as an input, the HOST Module **shall** leave the pins meant for the unused voltages as Reserved.

5.1.1 HOST Plug-In Module Requirements

T2-RUL-0053: HOST Plug-In Modules **shall** follow ANSI/VITA 46.0, Rule 3-1 regarding safety ground.

T2-RUL-0054: HOST Plug-In Modules **shall** follow ANSI/VITA 46.0, Rule 3-15 regarding dielectric separation.

T2-RUL-0057: HOST Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.9 3.3V_AUX.

T2-RUL-0058: HOST Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.11 SYSRESET*.

T2-RUL-0059: HOST Plug-In Modules **shall** draw no more than 1 mA from VBAT per Rule 4-56.1 of ANSI/VITA 46.0.

T2-RUL-0061: If implementing the 12V_AUX +/-, HOST Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.10 12V_AUX.

5.1.1.1 Payload Modules

5.1.1.1.1 Common 6U and 3U Payload Module Requirements

This Tier 2 HOST Standard utilizes one set of HOST-defined OpenVPX slot and *Module Profiles* for all HOST Payload Modules. The *Slot Profile* maps specific OpenVPX module connections to the HOST System Communications, System I/O, Chassis Management, and System Power Transmission Interfaces made available at the HOST Backplane. The Module Profile specifies serial channel baud rates. HOST Payload Modules are a type of HOST Plug-In Module.

T2-RUL-0140: Payload Modules **shall** conform to the interface requirements of the SCTI per SECTION 5.4.1.2.

T2-RUL-0055: Payload Modules **shall** be designed to accommodate any combination of power supply power up and power down sequences without causing board failure.

T2-RUL-0056: Payload Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.3 System Controller.

T2-REC-0010: When single-ended user defined signals that require tight tolerances, precise values, and/or very short rise times, are routed over pins intended for differential pairs, just the positive pin of a

pair **should** be used for the signal, with the negative pin of the pair grounded. This is to prevent potential crosstalk of the single-ended user defined signals.

T2-OBS-0080: The SPDI supports the battery backup power rail per ANSI/VITA 65.0, Section 3.2.2 and ANSI/VITA 46.0, section 4.9.2.

T2-OBS-0081: Refer to recommendations of ANSI/VITA 65.0, Section 3.2.4 on inrush (surge) current.

T2-RUL-0240: Payload Modules **shall** implement the requirements of ANSI/VITA 65.0, 6.3.3, (User Defined).

T2-OBS-0150: The OpenVPX User Defined connections are part of the SIOTI as defined in SECTION 5.4.1.3.

T2-PER-0039: Payload Modules **may** utilize a newer generation of *Peripheral Component Interconnect Express* (PCIe) than what is called out in the Module Profile.

5.1.1.1.1.1 Common Payload Module with Mezzanine Site Requirements

T2-RUL-0080: Payload Modules with PMC mezzanine sites **shall** conform to the carrier board, referred to as a host board in IEEE 1386.1, requirements of IEEE 1386.1.

T2-RUL-0090: Payload Modules with XMC mezzanine sites **shall** conform to the carrier board requirements of ANSI/VITA 42.0, XMC.

T2-OBS-0010: Compatibility with the PMC/XMC communications protocols is defined by the SCTI in SECTION 5.4.1.2.

T2-OBS-0020: Compatibility with the PMC/XMC power interfaces is defined by the SPDI in SECTION 5.4.1.6.

T2-OBS-0030: It is possible for a single mezzanine site to be compatible with both XMC and PMC mezzanine formats.

T2-OBS-0040: Mezzanine connector pinout requirements for Payload Modules with PMC Mezzanine sites are specified by IEEE Std. 1386.1 Section 5.2.

T2-OBS-0050: Voltage keying requirements for Payload Modules with PMC Mezzanine sites are specified by IEEE Std. 1386.1 Section 4.2.

T2-OBS-0060: Mezzanine connector pinout requirements for Payload Modules with XMC Mezzanine sites are specified by ANSI/VITA 42.0 Section 5-1.

T2-OBS-0070: It is possible for Payload Modules to be mezzanine carriers that do not natively contain any resources. In those cases, the Payload Module may only contain the bridges required to attach the PMC/XMC modules to the SCTI and CMTI.

T2-RUL-0100: Payload Module mezzanine sites configured to support a XMC Mezzanine **shall** implement the secondary XMC connector ground pins in accordance with ANSI/VITA 42.0 Table 5-4, Secondary XMC Connector Pin Definition, even if the signals of the Secondary connector are not used.

5.1.1.1.2 6U Payload Module Requirements

T2-RUL-0070: 6U Payload Modules **shall** conform to the 6U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0051: 6U Payload Modules **shall** follow ANSI/VITA 65.0, Section 12.1.2 with regards to Power Voltages and System Management.

T2-OBS-0079: Refer to ANSI/VITA 65.0, Recommendation 12.1.1.2-1 regarding maximum module power draw.

T2-RUL-0251: 6U Payload Modules **shall** conform to 6U Payload Profile 1, SECTION 5.1.1.1.2.1.

5.1.1.1.2.1 6U Payload Profile 1: PAY-4F1Q2U2T

T2-RUL-0249: 6U Payload Profile 1 Modules **shall** conform to the Slot Profile SLT6-PAY-4F1Q2U2T-10.2.1 per ANSI/VITA 65.0, Section 10.2.1.

T2-OBS-0100: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0101: The OpenVPX Expansion Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-RUL-0200: If a 6U Payload Profile 1 Module implements the Control Plane thin pipes, a Payload Module **shall** use the Control Plane thin pipes exclusively as part of the SIOTI.

T2-REC-0001: 6U Payload Profile 1 Modules **should** use the Control Plane thin pipes for debug.

T2-OBS-0110: The OpenVPX Control Plane is part of the CMTI as defined in SECTION 5.4.1.5.

T2-OBS-0111: The *Ultra-Thin Pipes* (UTP) of the OpenVPX Control Plane are also part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0120: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0250: 6U Payload Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-PAY-4F1Q2U2T-12.2.1-8
- MOD6-PAY-4F1Q2U2T-12.2.1-14
- MOD6-PAY-4F1Q2U2T-12.2.1-15
- MOD6-PAY-4F1Q2U2T-12.2.1-19

T2-PER-0045: 6U Payload Profile 1 Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0062: 6U Payload Profile 1 Modules using 10GBASE-KR **shall** comply with ANSI/VITA 65.0, Section 5.1.7.

5.1.1.1.2.2 6U Payload Module with Mezzanine Site Requirements

T2-RUL-0110: 6U Payload Module mezzanine sites configured to exclusively support a PMC Mezzanine **shall** conform to ANSI/VITA 46.9, Section 5.1 (P64S) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0120: 6U Payload Module mezzanine sites configured to exclusively support a XMC Mezzanine **shall** conform to ANSI/VITA 46.9, Section 5.4 (X38S+X8D+X12D) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0130: 6U Payload Module mezzanine sites configured to support both PMC and XMC Mezzanines **shall** conform to ANSI/VITA 46.9, Section 5.2 (P64S+X12D) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

5.1.1.1.2.3 6U HOST Payload Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements

T2-PER-0046: 6U Payload Modules **may** replace the P3 and P6 connectors with a blind mate connector compliant to ANSI/VITA 66.0 or ANSI/VITA 67.0 and their related dot standard.

T2-RUL-0132: If following Permission 0046, 6U Payload Modules **shall** conform to one of the following slot profiles per ANSI/VITA 65.1:

- SLT6-PAY-4F1Q1H2U2T1H-10.6.1-n

T2-OBS-0148: HOST only defines the aperture type and location and not the specific connector. The H aperture takes ANSI/VITA 67.3 type C connector modules.

5.1.1.1.3 3U Payload Module Requirements

T2-RUL-0142: 3U Payload Modules **shall** conform to the 3U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0141: 3U Payload Modules **shall** follow ANSI/VITA 65.0, Section 16.1.2 with regards to Power Voltages and System Management.

T2-OBS-0154: Refer to ANSI/VITA 65.0, Recommendation 16.1.1.2-1 regarding maximum module power draw.

T2-RUL-0159: 3U Payload Modules **shall** conform to one of the 3U Payload Profiles called out in the 5.1.1.1.3 subsections below.

5.1.1.1.3.1 3U Payload Profile 1: PAY-2F2U

T2-RUL-0160: 3U Payload Profile 1 Modules **shall** conform to the Slot Profile SLT3-PAY-2F2U-14.2.3 per ANSI/VITA 65.0, Section 14.2.3.

T2-OBS-0155: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0156: The OpenVPX Control Plane is part of both the SCTI and CMTI as defined in SECTION 5.4.1.2 and SECTION 5.4.1.5.

T2-OBS-0157: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0161: 3U Payload Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-2F2U-16.2.3-3
- MOD3-PAY-2F2U-16.2.3-5
- MOD3-PAY-2F2U-16.2.3-10
- MOD3-PAY-2F2U-16.2.3-11

T2-PER-0050: 3U Payload Profile 1 Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

T2-PER-0051: 3U Payload Profile 1 Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0147: 3U Payload Profile 1 Modules using 10GBASE-KR **shall** comply with ANSI/VITA 65.0, Section 5.1.7.

T2-RUL-0157: 3U Payload Profile 1 Modules with backplane USB interfaces **shall** populate pins for one USB interface in accordance with the USB usage defined in TABLE 5-2 and Table 5-3.

T2-RUL-0158: 3U Payload Profile 1 Modules with backplane SATA (Serial Advanced Technology Attachment) interfaces **shall** populate pins for one SATA interface in accordance with the SATA interface defined in TABLE 5-2 and TABLE 5-3.

T2-RUL-0179: 3U Payload Profile 1 Modules with backplane DisplayPort interfaces **shall** populate pins for one DisplayPort interface in accordance with the DisplayPort interface defined in TABLE 5-2 and Table 5-3.

5.1.1.1.3.2 3U Payload Profile 2: PAY-1F1F2U

T2-RUL-0162: 3U Payload Profile 2 Modules **shall** conform to the Slot Profile SLT3-PAY-1F1F2U-14.2.4 per ANSI/VITA 65.0, Section 14.2.2.

T2-OBS-0162: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0163: The OpenVPX Expansion Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0164: The OpenVPX Control Plane is part of both the SCTI and CMTI as defined in SECTION 5.4.1.2 and SECTION 5.4.1.5.

T2-OBS-0165: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0163: 3U Payload Profile 2 Modules **shall** conform to the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-1F1F2U-16.2.4-8

T2-PER-0055: 3U Payload Profile 2 Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

T2-PER-0056: 3U Payload Profile 2 Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0164: 3U Payload Profile 2 Modules using 10GBASE-KR **shall** comply with ANSI/VITA 65.0, Section 5.1.7.

T2-RUL-0165: 3U Payload Profile 2 Modules with backplane USB interfaces **shall** populate pins for one USB interface in accordance with the USB usage defined in TABLE 5-2 and TABLE 5-3.

T2-RUL-0166: 3U Payload Profile 2 Modules with backplane SATA interfaces **shall** populate pins for one SATA interface in accordance with the SATA interface defined in TABLE 5-2 and TABLE 5-3.

T2-RUL-0167: 3U Payload Profile 2 Modules with backplane DisplayPort interfaces **shall** populate pins for one DisplayPort interface in accordance with the DisplayPort interface defined in Table 5-2 and TABLE 5-3.

5.1.1.1.3.3 3U Payload Profile 3: PAY-1F1F1F2S1U2U1U1S1U1T1F

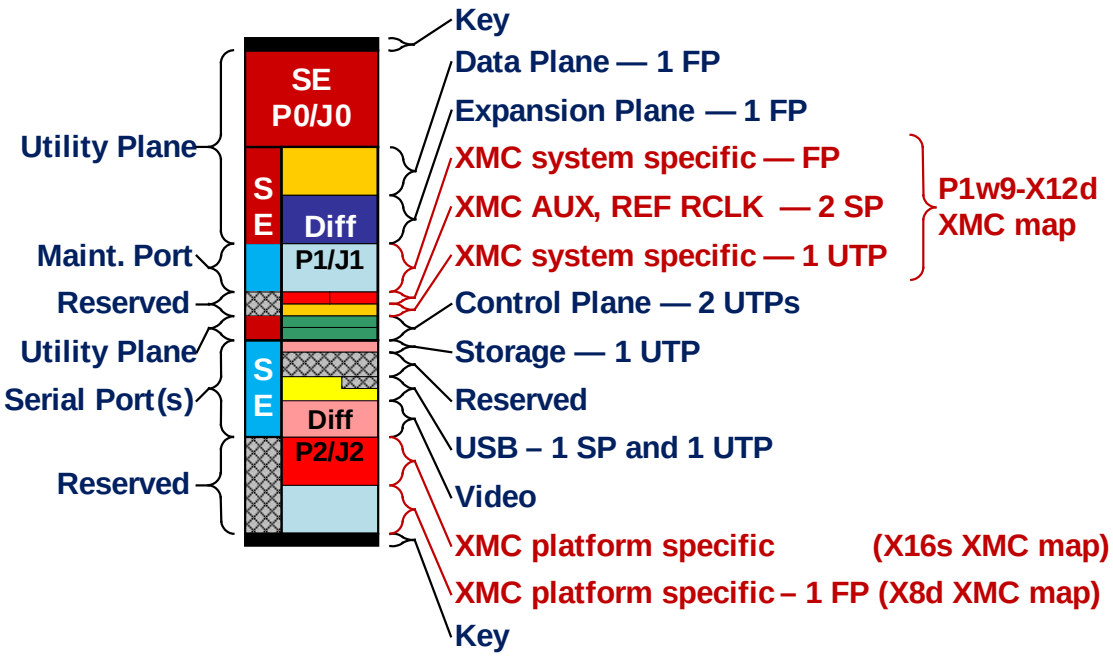

Figure 5.1-2 – SLT3-PAY-1F1F1F2S1U2U1U1S1U1T1F

T2-RUL-0168: The Utility Plane pins on P0/J0 **shall** be implemented as described in TABLE 3.7-1 and Table 3.7-2 of ANSI/VITA 65.0, and TABLE 5-1 of this document for single ended pins of P1/J1.

T2-RUL-0169: The Data Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document, with usage complying with section 6.2.2 of ANSI/VITA 65.0.

T2-RUL-0170: The Expansion Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document, with usage complying with section 6.2.2 of ANSI/VITA 65.0.

T2-RUL-0171: The Control Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document, with usage complying with section 6.2.2 of ANSI/VITA 65.0.

T2-RUL-0172: The XMC pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document.

T2-RUL-0173: The XMC pins on P2/J2 **shall** be implemented as described in TABLE 5-2 of this document.

T2-RUL-0174: The USB pins on P2/J2 **shall** be implemented as described in TABLE 5-2 of this document.

T2-RUL-0175: The storage pins on P2/J2 **shall** be implemented as described in TABLE 5-2 of this document.

T2-RUL-0176: The video pins on P2/J2 **shall** be implemented as described in TABLE 5-2 of this document.

Table 5-1 Payload Slot Profile SLT3-PAY-1F1F1F2S1U2U1U1S1U1T1F - P1 & J1

Plug-in module P1			Row G	Row F	Row E		Row D	Row C	Row B		Row A
					Even	Odd			Even	Odd	
Bplane J1			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	DP Port 1	X8 x4 / 2x2 / 4x1	GDiscrete1	GND	*GND-J1*	DP01-TD0-	DP01-TD0+	GND	*GND-J1*	DP01-RD0-	DP01-RD0+
2			GND	DP01-TD1-	DP01-TD1+	*GND-J1*	GND	DP01-RD1-	DP01-RD1+	*GND-J1*	GND
3			P1-VBAT	GND	*GND-J1*	DP01-TD2-	DP01-TD2+	GND	*GND-J1*	DP01-RD2-	DP01-RD2+
4			GND	DP01-TD3-	DP01-TD3+	*GND-J1*	GND	DP01-RD3-	DP01-RD3+	*GND-J1*	GND
5	EP Port 1	X8 x4 / 2x2 / 4x1	SYS_CON*	GND	*GND-J1*	EP01-TD0-	EP01-TD0+	GND	*GND-J1*	EP01-RD0-	EP01-RD0+
6			GND	EP01-TD1-	EP01-TD1+	*GND-J1*	GND	EP01-RD1-	EP01-RD1+	*GND-J1*	GND
7			Reserved	GND	*GND-J1*	EP01-TD2-	EP01-TD2+	GND	*GND-J1*	EP01-RD2-	EP01-RD2+
8			GND	EP01-TD3-	EP01-TD3+	*GND-J1*	GND	EP01-RD3-	EP01-RD3+	*GND-J1*	GND
9	XMC Fat Pipe		MP01-TD	GND	*GND-J1*	XMCfp-T0-	XMCfp-T0+	GND	*GND-J1*	XMCfp-R0-	XMCfp-R0+
10			GND	XMCfp-T1-	XMCfp-T1+	*GND-J1*	GND	XMCfp-R1-	XMCfp-R1+	*GND-J1*	GND
11			MP01-RD	GND	*GND-J1*	XMCfp-T2-	XMCfp-T2+	GND	*GND-J1*	XMCfp-R2-	XMCfp-R2+
12			GND	XMCfp-T3-	XMCfp-T3+	*GND-J1*	GND	XMCfp-R3-	XMCfp-R3+	*GND-J1*	GND
13	XMC Clocks		RSVD	GND	*GND-J1*	XMC_AUX_ RCLK-	XMC_AUX_ RCLK+	GND	*GND-J1*	XMC_REF_ RCLK-	XMC_REF_ RCLK+
14	XMC utp		GND	XMCutp-T-	XMCutp-T+	*GND-J1*	GND	XMCutp-R-	XMCutp-R+	*GND-J1*	GND
15	Control Plane		Maskable Reset*	GND	*GND-J1*	CPutp02-TD-	CPutp02-TD+	GND	*GND-J1*	CPutp02-RD-	CPutp02-RD+
16			GND	CPutp01-TD-	CPutp01-TD+	*GND-J1*	GND	CPutp01-RD-	CPutp01-RD+	*GND-J1*	GND

Table 5-2 Payload Slot Profile 1F1F1F2S1U2U1U1S1U1T1F - P2 & J2

Plug-In Mod P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Store UTP	SER01-TX-	GND	*GND-J2*	STRutp01-TD-	STRutp01-TD+	GND	*GND-J2*	STRutp01-RD-	STRutp01-RD+
2	RSVD	GND	Reserved	Reserved	*GND-J2*	GND	Reserved	Reserved	*GND-J2*	GND
3		SER01-TX+	GND	*GND-J2*	Reserved	Reserved	GND	*GND-J2*	Reserved	Reserved
4	USB, RSVD	GND	USB01-D-	USB01-D+	*GND-J2*	GND	USB01-VBUS	Reserved	*GND-J2*	GND
5		SER01-RX-	GND	*GND-J2*	USB01-SST-	USB01-SST+	GND	*GND-J2*	USB01-SSR-	USB01-SSR+
6	Video	GND	VID01-D0-	VID01-D0+	*GND-J2*	GND	VID01-D1-	VID01-D1+	*GND-J2*	GND
7		SER01-RX+	GND	*GND-J2*	VID01-D2-	VID01-D2+	GND	*GND-J2*	VID01-D3-	VID01-D3+
8		GND	VID01-SCL	VID01-SDA	*GND-J2*	GND	VID01-HPD	VID01-PWR	*GND-J2*	GND
9	X16s XMC map	RSVD	GND	*GND-J2*	Jn6-C12	Jn6-C13	GND	*GND-J2*	Jn6-F12	Jn6-F13
10		GND	Jn6-C14	Jn6-C15	*GND-J2*	GND	Jn6-F14	Jn6-F15	*GND-J2*	GND
11		RSVD	GND	*GND-J2*	Jn6-C16	Jn6-C17	GND	*GND-J2*	Jn6-F16	Jn6-F17
12		GND	Jn6-C18	Jn6-C19	*GND-J2*	GND	Jn6-F18	Jn6-F19	*GND-J2*	GND
13	X8d XMC map	RSVD	GND	*GND-J2*	Jn6-A1	Jn6-B1	GND	*GND-J2*	Jn6-D1	Jn6-E1
14		GND	Jn6-A3	Jn6-B3	*GND-J2*	GND	Jn6-D3	Jn6-E3	*GND-J2*	GND
15		RSVD	GND	*GND-J2*	Jn6-A11	Jn6-B11	GND	*GND-J2*	Jn6-D11	Jn6-E11
16		GND	Jn6-A13	Jn6-B13	*GND-J2*	GND	Jn6-D13	Jn6-E13	*GND-J2*	GND

T2-OBS-0051: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0052: The OpenVPX Control Plane is part of both the SCTI and CMTI as defined in SECTION 5.4.1.2 and SECTION 5.4.1.5.

T2-OBS-0053: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0177: 3U Payload Profile 3 Modules **shall** conform to one of the following Module Profiles listed in TABLE 5-3.

T2-PER-0002: 3U Payload Profile 3 Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

Table 5-3 Payload Module Profiles MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1F

Module Profile	Protocols for Copper Planes			Miscellaneous Protocols over copper connectors					
	Data Plane	Expansion Plane	Control Plane						
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1F	**DP01**	**EP01**	**CPutp01,CPutp02**	**STRutp01**	**USB01**	**Video**	**XMC Platform specific FP: XMCfp**	**Radial CLK termination type: XMC_AUX_RCLK XMC_REF_RCLK**	**XMC Platform specific UTP: XMCutp**
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1F-1	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1F-2	10GBASE-KX4 - per ANSI/VITA 65.0, Section 5.1.5	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1F-3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1F-4	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	10GBase-KR - per ANSI/VITA 65.0, Section 5.1.7	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	10GBase -KR - per ANSI/VITA 65.0, Section 5.1.7

5.1.1.1.3.4 3U Payload Profile 4: PAY-1F1F1F2S1U2U1U1S1U1T1J

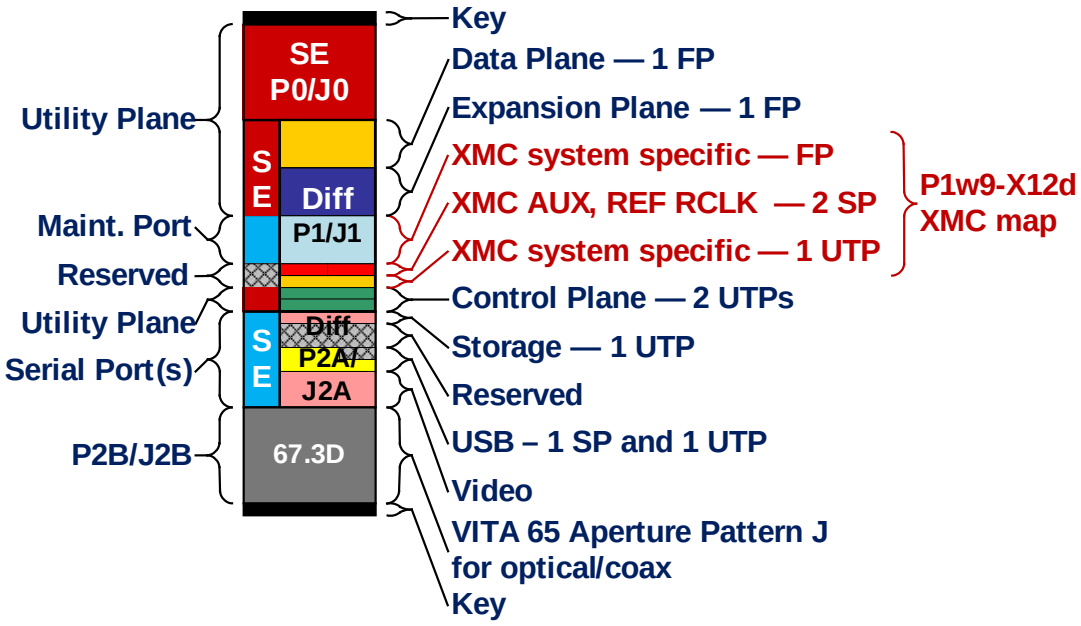

Figure 5.1-3 – SLT3-PAY-1F1F1F2S1U2U1U1S1U1T1J

T2-RUL-0091: The Utility Plane pins on P0/J0 **shall** be implemented as described in Table 3.7-1 and Table 3.7-2 of ANSI/VITA 65.0, and Table 5-4 of this document for single ended pins of P1/J1.

T2-RUL-0092: The Data Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-4 of this document, with usage complying with section 6.2.2 of ANSI/VITA 65.0.

T2-RUL-0093: The Expansion Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-4 of this document, with usage complying with section 6.2.2 of ANSI/VITA 65.0.

T2-RUL-0094: The Control Plane pins on P1/J1 **shall** be implemented as described in Table 5-4 of this document, with usage complying with section 6.2.2 of ANSI/VITA 65.0.

T2-RUL-0095: The XMC pins on P1/J1 **shall** be implemented as described in Table 5-4 of this document.

T2-RUL-0096: The USB pins on P2/J2 **shall** be implemented as described in Table 5-5 of this document.

T2-RUL-0097: The storage pins on P2/J2 **shall** be implemented as described in Table 5-5 of this document.

T2-RUL-0098: The video pins on P2/J2 **shall** be implemented as described in Table 5-5 of this document.

Table 5-4 Payload Slot Profile SLT3-PAY-1F1F1F2S1U2U1U1S1U1T1J - P1 & J1

Plug-in module P1				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	DP Port 1	X8	x4 / 2x2 / 4x1	GDiscrete1	GND	*GND-J1*	DP01-TD0-	DP01-TD0+	GND	*GND-J1*	DP01-RD0-	DP01-RD0+
2				GND	DP01-TD1-	DP01-TD1+	*GND-J1*	GND	DP01-RD1-	DP01-RD1+	*GND-J1*	GND
3				P1-VBAT	GND	*GND-J1*	DP01-TD2-	DP01-TD2+	GND	*GND-J1*	DP01-RD2-	DP01-RD2+
4				GND	DP01-TD3-	DP01-TD3+	*GND-J1*	GND	DP01-RD3-	DP01-RD3+	*GND-J1*	GND
5	EP Port 1		x4 / 2x2 / 4x1	SYS_CON*	GND	*GND-J1*	EP01-TD0-	EP01-TD0+	GND	*GND-J1*	EP01-RD0-	EP01-RD0+
6				GND	EP01-TD1-	EP01-TD1+	*GND-J1*	GND	EP01-RD1-	EP01-RD1+	*GND-J1*	GND
7				Reserved	GND	*GND-J1*	EP01-TD2-	EP01-TD2+	GND	*GND-J1*	EP01-RD2-	EP01-RD2+
8				GND	EP01-TD3-	EP01-TD3+	*GND-J1*	GND	EP01-RD3-	EP01-RD3+	*GND-J1*	GND
9	XMC Fat Pipe			MP01-TD	GND	*GND-J1*	XMCfp-T0-	XMCfp-T0+	GND	*GND-J1*	XMCfp-R0-	XMCfp-R0+
10				GND	XMCfp-T1-	XMCfp-T1+	*GND-J1*	GND	XMCfp-R1-	XMCfp-R1+	*GND-J1*	GND
11				MP01-RD	GND	*GND-J1*	XMCfp-T2-	XMCfp-T2+	GND	*GND-J1*	XMCfp-R2-	XMCfp-R2+
12				GND	XMCfp-T3-	XMCfp-T3+	*GND-J1*	GND	XMCfp-R3-	XMCfp-R3+	*GND-J1*	GND
13	XMC Clocks			RSVD	GND	*GND-J1*	XMC_AUX_ RCLK-	XMC_AUX_ RCLK+	GND	*GND-J1*	XMC_REF_ RCLK-	XMC_REF_ RCLK+
14	XMC utp			GND	XMCutp-T-	XMCutp-T+	*GND-J1*	GND	XMCutp-R-	XMCutp-R+	*GND-J1*	GND
15	Control Plane			Maskable Reset*	GND	*GND-J1*	CPutp02-TD-	CPutp02-TD+	GND	*GND-J1*	CPutp02-RD-	CPutp02-RD+
16				GND	CPutp01-TD-	CPutp01-TD+	*GND-J1*	GND	CPutp01-RD-	CPutp01-RD+	*GND-J1*	GND

Table 5-5 Payload Slot Profile SLT3-PAY-1F1F1F2S1U2U1U1S1U1T1J - P2 & J2

Plug-In Mod P2A		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J2A		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Store UTP	SER01-TX-	GND	*GND-J2*	STRupt01-TD-	STRupt01-TD+	GND	*GND-J2*	STRutp01-RD-	STRutp01-RD+
2	RSV	GND	Reserved	Reserved	*GND-J2*	GND	Reserved	Reserved	*GND-J2*	GND
3		SER01-TX+	GND	*GND-J2*	Reserved	Reserved	GND	*GND-J2*	Reserved	Reserved
4	USB, RSV	GND	USB01-D-	USB01-D+	*GND-J2*	GND	USB01-VBUS	Reserved	*GND-J2*	GND
5		SER01-RX-	GND	*GND-J2*	USB01-SST-	USB01-SST+	GND	*GND-J2*	USB01-SSR-	USB01-SSR+
6	Video	GND	VID01-D0-	VID01-D0+	*GND-J2*	GND	VID01-D1-	VID01-D1+	*GND-J2*	GND
7		SER01-RX+	GND	*GND-J2*	VID01-D2-	VID01-D2+	GND	*GND-J2*	VID01-D3-	VID01-D3+
8		GND	VID01-SCL	VID01-SDA	*GND-J2*	GND	VID01-HPD	VID01-PWR	*GND-J2*	GND

T2-OBS-0054: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0055: The OpenVPX Control Plane is part of both the SCTI and CMTI as defined in SECTION 5.4.1.2 and section 5.4.1.5.

T2-OBS-0056: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0099: 3U Payload Profile 4 Modules **shall** conform to one of the following Module Profiles listed in TABLE 5-1.

T2-PER-0081: 3U Payload Profile 4 Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

T2-RUL-0291: 3U Payload Modules **shall** populate the P2 connector with a blind mate connector compliant to ANSI/VITA 66.0 or ANSI/VITA 67.0 and their related dot standard.

Table 5-6 Payload Module Profiles MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1J

Module Profile	Protocols for Copper Planes			Miscellaneous Protocols over copper connectors						Protocols for Optical
	Data Plane	Expansion Plane	Control Plane							
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1J	**DP01**	**EP01**	**CPutp01,CPutp02**	**STRutp01**	**USB01**	**Video**	**XMC Platform specific FP: XMCfp**	**Radial CLK termination type: XMC_AUX_RCLK XMC_REF_RCLK**	**XMC Platform specific UTP: XMCutp**	
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1J-1	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1J-2	10GBASE-KX4 - per ANSI/VITA 65.0, Section 5.1.5	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1J-3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	
MOD3-PAY-1F1F1F2S1U2U1U1S1U1T1J-4	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	10GBase-KR - per ANSI/VITA 65.0, Section 5.1.7	SATA Gen 3 - per ANSI/VITA 65.0, Section 5.6.3	USB 3.1 Gen 1 - per USB 3.1 Specification	DisplayPort 1.2 - per DisplayPort Standard Specification Ver. 1.2	User Defined	Parallel	10GBase -KR - per ANSI/VITA 65.0, Section 5.1.7	

5.1.1.1.3.5 3U Payload Profile 5: PER-1U (Reserved for use as Dedicated I/O Module)

Payload Profile 5 is meant only for an I/O dedicated module acting as an interface between platform specific I/O over the User Defined (UD) pins and processing modules over the Ultra-Thin Pipe. It maximizes the number of UD pins to enable the module to interface with a maximum quantity of platform I/O. Payload Profile 5 is not meant to be used for processing resources such as a Single Board Computer or Data Processor. The purpose of this module is to allow a system designer to have a central hub for all platform specific I/O and thus only use standardized signals on modules within the System.

T2-RUL-0292: 3U Payload Profile 5 Modules **shall** conform to the Slot Profile SLT3-PER-1U per ANSI/VITA 65.0, Section 14.3.3.

T2-OBS-0057: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0058: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0293: 3U Payload Profile 5 Modules **shall** conform to the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PER-1U-16.3.3-2
- MOD3-PER-1U-16.3.3-3

5.1.1.1.3.6 3U Payload Module with Mezzanine Site Requirements

T2-RUL-0148: 3U Payload Module mezzanine sites configured to exclusively support a PMC Mezzanine **shall** conform to ANSI/VITA 46.9, Section 4.1 (P64S) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0149: 3U Payload Module mezzanine sites configured to exclusively support a XMC Mezzanine **shall** conform to one of the following options regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector if not defined by the payload profile:

1. ANSI/VITA 46.9, Section 4.4, X24S+X8D+X12D.
2. ANSI/VITA 46.9, Section 4.8, X12D.

T2-RUL-0151: 3U Payload Module mezzanine sites configured to support both PMC and XMC Mezzanines **shall** conform to ANSI/VITA 46.9, Section 4.2 (X12D+P64S) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector

5.1.1.1.3.7 3U HOST Payload Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements

T2-PER-0054: 3U Payload Modules **may** replace the P2 connector with a blind mate connector compliant to ANSI/VITA 66.0 or ANSI/VITA 67.0 and their related dot standard.

T2-RUL-0152: If following Permission 0054, 3U Payload Modules **shall** conform to one of the following slot profiles per ANSI/VITA 65.1:

- SLT3-PAY-2F2U1J-14.6.9-n

T2-OBS-0147: HOST only defines the aperture type and location and not the specific connector. The J aperture takes ANSI/VITA 67.3 type D connector modules.

5.1.1.2 Power Supply Modules

5.1.1.2.1 Common 6U and 3U Power Supply Module Requirements

T2-RUL-0310: PSM requirements **shall** be applied using the following order of precedence:

1. Requirements of this Tier 2 HOST Standard (including additions or exclusions to ANSI/VITA 65.0)
2. Requirements of ANSI/VITA 62.0

T2-OBS-0170: PSMs can be configured as a single-stage or two-stage power supply system as specified by ANSI/VITA 62.0, Section 1.2.

T2-OBS-0180: PSMs can utilize energy storage modules as specified by ANSI/VITA 62.0 to satisfy Target System power hold-up requirements.

T2-RUL-0320: PSMs **shall** assert the FAIL* signal when PO1, PO2, PO3, or AUX voltages are not within their voltage specifications per ANSI/VITA 62.0, Recommendation 3.3-2.

T2-RUL-0330: PSMs that accept external prime input power **shall** do so in accordance with ANSI/VITA 62.0, Section 6.5.1.

T2-OBS-0190: PSMs that accept external prime input power include Single-Stage Power Subsystem Modules and Front-End Modules of Two-Stage Power Subsystems.

T2-RUL-0340: PSMs that supply power to the payload/switch slot portion of the HOST Backplane **shall** output +12V final power in accordance with ANSI/VITA 62.0, Section 4.6.1.2 and Section 4.6.1.1.1.

T2-RUL-0350: PSMs that supply power to the payload/switch slot portion of the HOST Backplane **shall** output +5V final power in accordance with ANSI/VITA 62.0, Section 4.6.1.5.

T2-RUL-0360: PSMs that supply power to the payload/switch slot portion of the HOST Backplane **shall** output 3.3V_AUX in accordance with ANSI/VITA 62.0, Section 4.6.1.7.

T2-RUL-0370: PSMs that supply power to the payload/switch slot portion of the HOST Backplane **shall** output +/-12V AUX in accordance with ANSI/VITA 62.0, Section 4.6.1.8.

T2-OBS-0200: PSMs supplying power to payloads/switches include Single-Stage Power Subsystem Modules and Back-End Modules of a Two-Stage Power Subsystem.

T2-OBS-0210: The ANSI/VITA 62.0 requirements for +48V final power are not applicable to this Tier 2 Core Technology Standard.

T2-RUL-0371: PSMs **shall** have the chassis pin connected to their front panel and covers.

T2-RUL-0372: PSMs **shall** have the chassis pin isolated from the SIGNAL_RETURN pin.

T2-RUL-0373: PSMs **shall** have the chassis pin isolated from power returns, such as the POWER_RETURN pins.

T2-RUL-0374: PSMs **shall** have the chassis pin isolated from the -DC_IN/ACN pin.

T2-OBS-0205: The rules for isolating the chassis pins come from ANSI/VITA 62.0, Recommendations in Section 4.7.

T2-RUL-0380: PSMs outputting an intermediate power **shall** explicitly define the nominal voltage level for the intermediate power.

T2-RUL-0390: PSMs having intermediate power as an input **shall** explicitly define the nominal voltage level for the intermediate power.

T2-OBS-0220: The SPDI is implemented using the OpenVPX Utility Plane as well as additional requirements specified herein.

T2-OBS-0230: PSMs make use of a subsection of the CMTI OpenVPX Utility Plane since they do not contain traditional processing elements.

T2-RUL-0391: PSMs **shall** conform to the requirements of ANSI/VITA 62.0 except where specified herein.

5.1.1.2.1.1 Common Energy Storage Module Requirements

T2-RUL-0480: Energy Storage Modules **shall** accept an input of the intermediate voltage in accordance with ANSI/VITA 62.0, Section 4.5.

T2-RUL-0490: Energy Storage Modules **shall** output the intermediate voltage in accordance with ANSI/VITA 62.0, Section 4.5.

5.1.1.2.2 6U Power Supply Module Requirements

T2-RUL-0300: 6U PSMs **shall** conform to the mechanical requirements of ANSI/VITA 48.2 for 6U conduction cooled modules except where specified herein.

5.1.1.2.2.1 6U Front-End Module Requirements

T2-OBS-0231: Requirements related to Front-End Modules are in ANSI/VITA 62.0 Section 4.6.2.1.2.

5.1.1.2.2.2 6U Back-End Module Requirements

T2-OBS-0232: Information and Requirements related to input of intermediate voltage are in ANSI/VITA 62.0 Section 4.6.2.2 and 6.5.1.

5.1.1.2.2.3 6U Single-Stage Module Requirements

T2-RUL-0500: 6U Single-Stage Modules **shall** route the intermediate voltage to the ANSI/VITA 62.0 pins labeled “POS_FILT_OUT” and “NEG_FILT_OUT” in accordance with ANSI/VITA 62.0, Section 6.5.2.

5.1.1.2.3 3U Power Supply Module Requirements

T2-RUL-0502: 3U PSMs **shall** conform to the mechanical requirements of ANSI/VITA 48.2 for 3U conduction cooled modules except where specified herein.

T2-RUL-0503: 3U PSMs that supply power to the payload/switch slot portion of the Backplane **shall** output +3.3V final power in accordance with ANSI/VITA 62.0, Section 4.6.1.4.

5.1.1.2.3.1 3U Front-End Module Requirements

T2-OBS-0233: Requirements related to Front-End Modules are in ANSI/VITA 62.0 Section 4.6.2.1.1.

5.1.1.2.3.2 3U Back-End Module Requirements

T2-OBS-0234: Information and Requirements related to input of intermediate voltage are in ANSI/VITA 62.0 Section 4.6.2.1 and Section 5.5.1.

5.1.1.3 Switch Modules

When using multiple Payload Modules, it is often necessary to utilize a Switch Module to accomplish the necessary communication.

5.1.1.3.1 Common 6U and 3U HOST Switch Requirements

T2-RUL-0531: Switch Modules **shall** implement the requirements of ANSI/VITA 65.0, Section 3.7 (OpenVPX ANSI/VITA 46.0 Connector P0/J0 and P1/J1 Connector Pin Assignments).

T2-RUL-0534: Switch Modules **shall** be designed to accommodate any combination of power supply power up and power down sequences without causing board failure.

T2-RUL-0535: Switch Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.3 System Controller and ANSI/VITA 65.0, Section 3.4.1.

T2-PER-0061: Switch Modules **may** implement 10GBASE-KR on the Control Plane UTPs.

T2-RUL-0511: Switch Modules using 10GBASE-KR **shall** comply with ANSI/VITA 65.0, Section 5.1.7.

T2-PER-0062: Switch Modules **may** combine Control Plane ultra-thin pipes to create Control Plane fat pipes.

T2-OBS-0237: It may be necessary to combine 4 10GBASE-KR ultra-thin pipes to create a single 40GBase-KR4 fat pipe.

T2-PER-0057: Switch Modules **may** utilize a newer generation of PCIe than what is called out in the Module Profile.

5.1.1.3.2 6U Switch Module Requirements

T2-RUL-0520: 6U Switch Modules **shall** be implemented as 6U OpenVPX Switch Plug-In Modules per SECTION 5.4.2.2.

T2-REC-0018: In order to allow their use in a Standard Development Chassis, 6U conduction-cooled Switch Modules **should** be designed to require ≤150W per slot.

T2-PER-0034: 6U conduction-cooled Switch Modules **may** be designed to require >150W per slot, but these modules might not be properly powered in a Standard Development Chassis.

T2-RUL-0533: 6U Switch Modules **shall** follow ANSI/VITA 65.0, Section 12.1.2 with regard to Power Voltages and System Management.

T2-RUL-0532: 6U Switch Modules **shall** conform to 6U Switch Profile 1, Section 5.1.1.3.2.1 or 6U Switch Profile 2, Section 5.1.1.3.2.2.

T2-RUL-0537: 6U Switch Modules **shall** conform to the 6U conduction-cooled requirements of ANSI/VITA 48.2.

5.1.1.3.2.1 6U Switch Profile 1: SWH-20U19F

T2-RUL-0540: 6U Switch Profile 1 Modules **shall** conform to the Slot Profile SLT6-SWH-20U19F-10.4.1 per ANSI/VITA 65.0, Section 10.4.1.

T2-RUL-0550: 6U Switch Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-SWH-20U19F-12.4.1-3
- MOD6-SWH-20U19F-12.4.1-5
- MOD6-SWH-20U19F-12.4.1-10
- MOD6-SWH-20U19F-12.4.1-15

T2-OBS-0238: Note that the MOD6-SWH-20U19F-12.4.1-3 switch has PCIe in the Data Plane, but this is the profile that would be used in a system that wants to utilize HOST Payload's PCIe Expansion Plane as a switched network. Due to the Expansion Plane being primarily used for adjunct modules, the OpenVPX ecosystem does not contain Expansion Plane Switch Modules.

5.1.1.3.2.2 6U Switch Profile 2: SWH-16U20F

T2-RUL-0560: 6U Switch Profile 2 Modules **shall** conform to the Slot Profile SLT6-SWH-16U20F-10.4.2 per ANSI/VITA 65.0, Section 10.4.2.

T2-RUL-0570: 6U Switch Profile 2 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-SWH-16U20F-12.4.2-3
- MOD6-SWH-16U20F-12.4.2-5
- MOD6-SWH-16U20F-12.4.2-11
- MOD6-SWH-16U20F-12.4.2-15

T2-OBS-0239: Note that the MOD6-SWH-16U20F-12.4.2-3 switch has PCIe in the Data Plane. This is the profile that would be used in a system that wants to utilize HOST Payload's PCIe Expansion Plane as a switched network. Due to the Expansion Plane being primarily used for adjunct Modules, the OpenVPX ecosystem does not contain Expansion Plane Switch Modules.

5.1.1.3.3 3U Switch Module Requirements

T2-RUL-0568: 3U Switch Modules **shall** be implemented as 3U OpenVPX Switch Plug-In Modules per SECTION 5.4.2.2.

T2-REC-0019: In order to allow their use in a Standard Development Chassis, 3U conduction-cooled Switch Modules **should** be designed to require ≤75W per slot.

T2-PER-0035: 3U conduction-cooled Switch Modules **may** be designed to require >75W per slot, but these modules might not be properly powered in a Standard Development Chassis.

T2-RUL-0571: 3U Switch Modules **shall** follow ANSI/VITA 65.0, Section 16.1.2 with regard to Power Voltages and System Management.

T2-RUL-0572: 3U Switch Modules **shall** conform to 3U Switch Profile 1, Section 5.1.1.3.3.1 or 3U Switch Profile 2, Section 5.1.1.3.3.2.

T2-RUL-0587: 3U Switch Modules **shall** conform to the 3U conduction-cooled requirements of ANSI/VITA 48.2.

5.1.1.3.3.1 3U Switch Profile 1: SWH-6F6U

T2-RUL-0573: 3U Switch Profile 1 Modules **shall** conform to the Slot Profile SLT3-SWH-6F6U-14.4.1 per ANSI/VITA 65.0, Section 14.4.1.

T2-RUL-0574: 3U Switch Profile 1 Modules **shall** implement the external connection thin pipe per ANSI/VITA 65.0, Section 14.4.1.4.1.

T2-RUL-0575: 3U Switch Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-SWH-6F6U-16.4.1-3
- MOD3-SWH-6F6U-16.4.1-5
- MOD3-SWH-6F6U-16.4.1-10
- MOD3-SWH-6F6U-16.4.1-11

T2-PER-0066: 3U Switch Profile 1 modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

5.1.1.3.3.2 3U Switch Profile 2: SWH-2F24U

T2-RUL-0576: 3U Switch Profile 2 Modules **shall** conform to the Slot Profile SLT3-SWH-2F24U-14.4.3 per section ANSI/VITA 65.0, Section 14.4.3.

T2-PER-0101: If an application requires more than 24 Ultra-Thin Pipes the P1 Fat Pipes of 3U Switch Profile 2 **may** be repartitioned into Ultra-Thin Pipes.

T2-RUL-0591: If only one of the two available Fat Pipes on P1 of the 3U Switch Profile 2 is repartitioned it **shall** be the Fat Pipe closer to P2.

T2-PER-0021: If more than 2 Fat-Pipes are needed, the UTPs, CPutp01 thru CPutp24, **may** be repartitioned into Fat Pipes.

T2-OBS-0241: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-RUL-0581: 3U Switch Profile 2 Modules **shall** conform to MOD3-SWH-2F24U-16.4.3-4 per TABLE 5-7.

Table 5-7 3U 2F24U Switch Module Profile

Module Profile	Slot Profile	CPutp01-CPutp24	CP01, CP02(FP)	Comments
MOD3-SWH-2F24U-16.4.3-4	SLT3-SWH-2F24U-14.4.3	10GBASE-KR -- 5.1.7, 40GBASE-KR4 -- 5.1.8	40GBASE-KR4 -- 5.1.8, 10GBASE-KR -- 5.1.7	Each port can be configured separately for 4 lanes of 10GBASE-KR or a single 40GBASE-KR4.

Note: Sections in TABLE 5-7 reference ANSI/VITA 65.0.

5.1.2 Mezzanine Requirements

5.1.2.1 Common Mezzanine Requirements

HOST Mezzanine Modules are HOST Modules that mount onto a HOST Payload Module. The two types of HOST Mezzanine form factors are PMC and XMC.

T2-RUL-0590: Requirements for HOST Mezzanine Modules **shall** be applied using the following order of precedence:

1. Requirements of this HOST Tier 2 Standard (including additions or exclusions to PMC/XMC standards)
2. Mezzanine Module requirements of IEEE 1386.1 and ANSI/VITA 42.0 for PMCs and XMCs respectively

T2-RUL-0600: HOST Mezzanine Modules **shall** perform all of their required I/O functions through their mezzanine connectors.

T2-OBS-0240: Some sections of the mezzanine card standards contain requirements for mezzanine card front panel I/O. These requirements are not applicable to this Tier 2 technology. This Tier 2 technology only utilizes mezzanine card I/O that pass through the mezzanine card connector.

T2-RUL-0610: HOST Mezzanine Modules **shall** conform to the interface requirements of the SCTI for Mezzanine Modules per SECTION 5.4.1.2.

T2-OBS-0250: The SCTI for PMCs is implemented using OpenVPX high-speed serial interconnects to *Peripheral Component Interconnect* (PCI) bridging as defined in SECTION 5.4.1.2.2

T2-OBS-0260: The CMTI for Mezzanines is implemented using the OpenVPX Utility Plane in conjunction with the appropriate mezzanine card standard defined in SECTION 5.4.1.5.

T2-OBS-0270: The SPDI for Mezzanines is implemented using the OpenVPX Utility Plane in conjunction with the appropriate mezzanine card standard defined in SECTION 5.4.1.6.

T2-PER-0070: A Mezzanine connector that has no signals routed to it **may** be left unpopulated.

T2-PER-0080: A Mezzanine connector **may** leave a user defined signal as a no connect if the signal is not implemented in the mezzanine design.

T2-REC-0011: 6U Payload Modules with only one Mezzanine site **should** use a mapping to P3 and P4.

T2-OBS-0242: By using P3 and P4 for T2-REC-0011, if optical and/or coax connections are used, P6 and possibly P5 would be used for this purpose.

5.1.2.2 XMC Mezzanine Requirements

T2-RUL-0620: XMC Mezzanines **shall** conform to the requirements of ANSI/VITA 42.0 Standard for Switched Mezzanine Cards (herein referred to as XMC).

T2-RUL-0650: XMC Mezzanines that do not require utilization of all available user I/O signals **shall** leave the remaining unused signals as no connects.

T2-REC-0012: The higher priority I/O signals of the XMC Mezzanine **should** populate pins in the following order of ANSI/VITA 46.9 patterns:

1. X12d
2. X8d
3. X24s
4. X38s

T2-OBS-0245: There will be instances where Payload Modules only route a portion of the XMC I/O to the HOST backplane connectors and by following the priority stated in T2-REC-0012, the chance that a high priority signal will not be routed to the Backplane is decreased.

5.1.2.3 PMC Mezzanine Requirements

T2-RUL-0660: PMC Mezzanines **shall** conform to the requirements of IEEE Std. 1386.1 Standard for PCI Mezzanine Cards (referred to as PMC).

T2-RUL-0690: PMC Mezzanines that do not require utilization of all available user I/O signals **shall** leave the remaining unused signals as no connects.

T2-RUL-0700: If a PMC Mezzanine is implementing a 64-bit PCI bus for PMC communication, a PMC Mezzanine **shall** populate a minimum of Pn1, Pn2, and Pn3.

T2-OBS-0243: Pn4 is an optional connector used only for User I/O in 64-bit PCI bus implementations of PMCs.

T2-RUL-0710: If a PMC Mezzanine is implementing a 32-bit PCI bus for PMC communication, a PMC Mezzanine **shall** populate a minimum of Pn1 and Pn2.

T2-OBS-0244: Pn3 and Pn4 are optional connectors used only for User I/O in 32-bit PCI bus implementations of PMCs.

5.2 Hardware System Management Option

T2-OBS-0289: Section 5.2 Hardware System Management is planned to be required in a future version of this standard.

T2-RUL-0286: SM[1..0] (IPMB-A) **shall** be electrically unconnected on Level B Conformant Modules.

T2-RUL-0287: SM[3..2] (IPMB-B) **shall** be electrically unconnected on Level B Conformant Modules.

T2-RUL-0288: Level A Conformant Modules **shall** utilize SM[1..0] (IPMB-A) and SM[3..2] (IPMB-B).

T2-OBS-0011: Level A and Level B Conformant Modules are specified in SECTION 4.1.4.

5.3 Hardware System Management

5.3.1 Hardware System Management Overview

The Hardware System Management extends ANSI/VITA 46.11 which in turn leverages both the IPMI standard and the PICMG Advanced TCA (ATCA) 3.0 standard. HOST provides additional functional requirements to ANSI/VITA 46.11 and IPMI. Hardware System Management provides the following capabilities:

- **Sensor Management** – temperature, voltage, system modes etc.
- **System/Module Inventory** – vendor identification, model number, serial number, revision identification, SW/FW revision information
- **System/Module Configuration** – parameter settings, policy settings
- **SW/FW Management** – load, sanitize, recovery
- **FRU Recovery** – reset a module, power cycle a module
- **Diagnostic Management** – initiate diagnostics, collect diagnostic results

HOST differentiates from ANSI/VITA 46.11 in that it provides further standardization for key interfaces, provides additional capabilities related to defense systems and takes into consideration the perspective of defense system developers and integrators.

The following are key differentiations from ANSI/VITA 46.11:

HOST provides further standardization to:

- The payload interface
- The Manager Redundancy Interface (MRI)
- The FRU Mode Sensor to provide system modes which are typically provided on military platforms
- The *Intelligent Platform Management Bus (IPMB)* speed.

5.3.2 Hardware System Management Architecture

Hardware System Management is hierarchical in nature with the System Manager at the highest level. A System Manager may communicate with the *Chassis Manager* at the subsequent level. The Chassis Manager will communicate with the Intelligent Platform Management Controllers (IPMC) at the lowest level. Consistent with 46.11, the System Manager implementation details are outside the scope of this standard. The System Manager is typically application level software which can request or command the Chassis Manager to gather chassis information or request or command an IPMC to gather local

information. The below diagram, FIGURE 5.3-1, shows additional interfaces such as the MRI and Payload Interface which are required by HOST.

For additional details in regards to the three logical layers in system management refer to ANSI/VITA 46.11 Section 1.2.3.1.

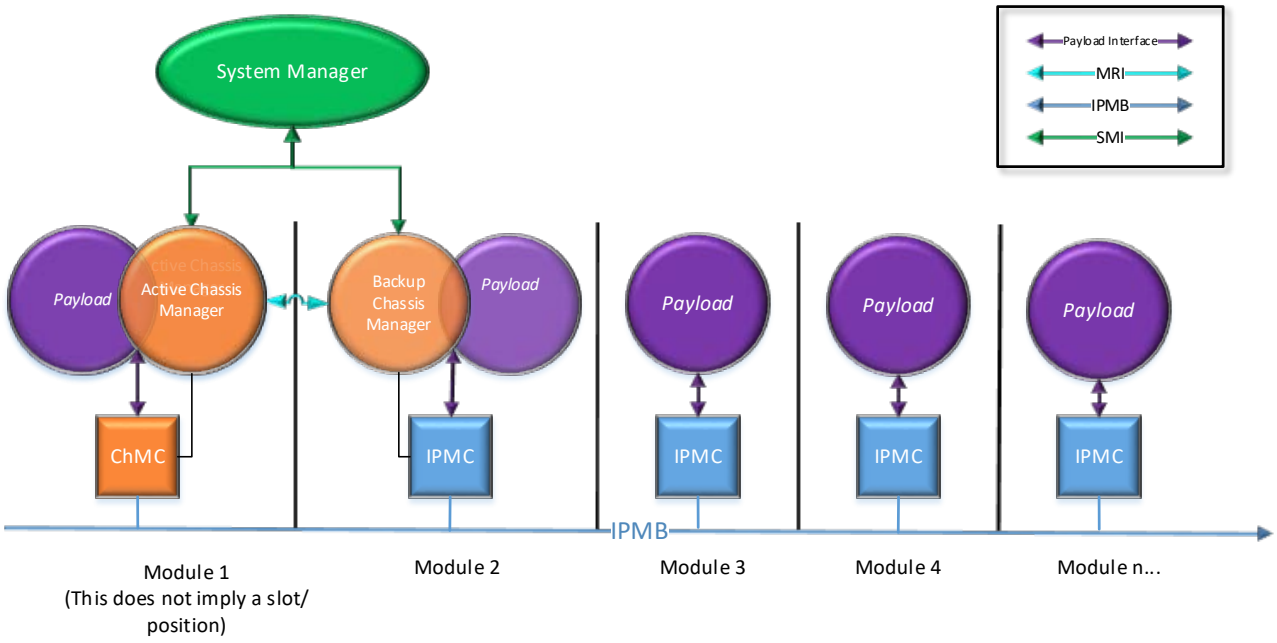

Figure 5.3-1 – Hardware System Management

5.3.3 Hardware System Management Requirements

T2-RUL-0295: Hardware System Management **shall** conform to the requirements of ANSI/VITA 46.11, including Tier-2 Chassis Manager and Tier-2 IPMC requirements.

T2-OBS-0059: ANSI/VITA 46.11 Section 8.2 defines requirements that will be utilized for the *Chassis Domain Inventory Information Record*. It is incumbent upon the integrator to determine the appropriateness and usefulness of populating the field for any particular design. The IPMI Platform Management FRU Information Storage Definition specification (Section 8, Common Header Format) provides guidance on how to indicate a particular FRU Record Area is not in use by setting the Starting Offset to 00h if the area is not present.

5.3.3.1 Chassis Manager

According to ANSI/VITA 46.11 a Chassis Manager is,

> *A logical entity in the VPX System Management architecture whose primary responsibility is to manage the IPMCs within a Chassis and provide a communication path between the System Manager and the aforementioned IPMCs. A Chassis Manager includes and can potentially be completely implemented on a Chassis Management Controller. The Chassis Manager is the middle level logical management layer in the VPX System Management architecture.*

The Chassis Manager communicates with IPMCs via the IPMB utilizing the IPMI protocol. The Tier 2 HOST Standard does not require or restrict the presence of multiple active Chassis Managers within a

physical chassis as long as each active Chassis Manager is connected to a separate IPMB. However, if there are *backup Chassis Managers* implemented on the same IPMB only one Chassis Manager should be active at any time, and it should use the MRI to communicate with a backup Chassis Manager.

The Chassis Manager provides a point of entry for the System Manager to join in managing the chassis, and interacting with the main aggregation of IPMC information.

The Chassis Manager is not required to be physically located on a specific HOST Module or other piece of hardware within the chassis, but can reside anywhere as specified by the Target System requirements.

T2-RUL-0720: Chassis Managers **shall** perform chassis management utilizing the system management bus pins SM[1..0] (IPMB-A) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-RUL-0285: Chassis Managers **shall** perform chassis management utilizing the system management bus pins SM[3..2] (IPMB-B) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-OBS-0280: The system management buses SM[3..0] represent the physical lines used for management communications. These data lines also make up a portion of the CMTI. See SECTION 5.4.1.5 for more details about the CMTI.

T2-RUL-0296: Chassis Managers **shall** support the System Manager Interface over Control Plane Ethernet within the Enclosure.

T2-OBS-0061: The System Manager Interface need not be connected to a Chassis Manager at any time but the Chassis Manager must fully support such connection when made.

T2-RUL-1940: Chassis Managers **shall** send a Set Event Receiver Message with the Event Receiver Slave Address field set to 20h upon entering an active state.

T2-OBS-0440: Chassis Managers are responsible for ensuring that all IPMCs on their IPMB have successfully received and processed the Set Event Receiver Message.

T2-OBS-0450: Setting the Event Receiver Slave Address to the Chassis Manager's address of 20h designates this address as the Event Receiver. See IPMI Section 29.1 for information on the Set Event Receiver Message.

T2-RUL-0822: Chassis Managers **shall** implement a System Event Log as defined in IPMI, Section 31 "System Event Log (SEL) Commands" and Section 32 "SEL Record Formats."

T2-RUL-0299: Chassis Manager Controllers (ChMCs) **shall** comply with the IPMC requirements for HOST.

5.3.3.2 Backup Chassis Manager

This standard recommends the use of a backup Chassis Manager. This section provides standardized requirements by which backup Chassis Managers perform communication to coordinate activities and achieve data coherency. It serves as a baseline for capability, performance, and interoperability and a toolset with which vendors and integrators may implement designs for redundancy. The active Chassis Manager sends messages on the IPMB using address 20h while backup Chassis Managers will only assume an active role if no messages from the active Chassis Manager are seen (or other failures of the active are observed).

T2-RUL-0301: There **shall** be only one active Chassis Manager in a HOST Chassis.

T2-OBS-0064: There is no requirement for a backup Chassis Manager to exist within a system.

T2-RUL-1101: The functional Chassis Manager with the lowest derived IPMB address **shall** be selected as active Chassis Manager.

T2-REC-0053: Chassis Managers **should** assume that they are not functional if a Chassis Manager with higher derived IPMB address indicates they are active.

T2-OBS-0062: The IPMB address reserved for the active Chassis Manager (20h) is not to be used for priority comparison.

T2-RUL-0303: Only the active Chassis Manager **shall** be enabled to send messages on the IPMB using address 20h.

T2-RUL-0304: Chassis Managers **shall** function as a backup Chassis Manager when another functioning Chassis Manager is active.

T2-OBS-0063: A backup Chassis Manager is a Chassis Manager operating in a backup state.

T2-PER-0023: Backup Chassis Managers **may** send or receive messages on the MRI and Payload Interface.

T2-PER-0024: Backup Chassis Managers **may** send or receive messages on the IPMB when functioning as an IPMC (not 20h).

T2-RUL-0305: Chassis Managers **shall** implement a MRI as a UDP/IP Multicast connection on IP address 224.0.0.224 and port 30101 for communication between all Chassis Managers in the chassis.

T2-OBS-0065: Chassis Managers are not required to have a physical connection to a backup Chassis Manager but must be able to operate with Ethernet if or when it is connected.

T2-RUL-1102: Active Chassis Managers **shall** send MRI messages (defined in 5.3.3.3) over the MRI at a minimum rate that is configurable from 1Hz to 100Hz.

T2-RUL-1103: Chassis Managers **shall** receive MRI messages over the MRI at a minimum rate that is configurable from 1Hz to 100Hz.

T2-REC-0021: Backup Chassis Managers **should** be configured with the same rate for a given chassis.

T2-OBS-0012: The previous two rules assume a functional, connected MRI.

T2-RUL-0307: A backup Chassis Manager **shall** take over as active Chassis Manager after an inactivity period that is a configurable multiple of messages not received based on the configured minimum message rate (i.e. N/rate in seconds).

T2-REC-0050: Chassis Managers **should** have accessible methods for updating configuration parameters to allow for different system requirements.

T2-PER-0025: This inactivity **may** be measured on the MRI, IPMB, or some combination of the two.

T2-REC-0022: The configured limit for consecutive messages not received **should** increase with IPMB address to help avoid contention for active Chassis Manager.

T2-REC-0023: A backup Chassis Manager **should** be capable of taking over as active Chassis Manager within three (3) seconds of detecting an active Chassis Manager failure.

T2-RUL-1104: When a Chassis Manager assumes an active role, it **shall** send a heartbeat message (including header and trailer specified in SECTION 5.3.3.3) indicating its active role before transmitting any other message.

T2-REC-0051: When a Chassis Manager assumes an active role, it **should** send a configuration message (including header and trailer specified in SECTION 5.3.3.3) to establish a known system state.

T2-REC-0027: The active Chassis Manager **should** forward Platform Event messages to backup Chassis Managers over the MRI.

T2-RUL-0308: When a Chassis Manager assumes an active role, it **shall** inherit and maintain all allocated ports and managed FRU status including FRU Records, Sensor Data Record (SDR), and SEL.

T2-RUL-1105: When an active Chassis Manager receives a heartbeat message indicating another Chassis Manager is active or an IPMB message with a transmit address of 20h it **shall** immediately transition to a backup state.

T2-OBS-0066: This should not happen unless multiple Chassis Managers are assuming they are active or are contending for active Chassis Manager. Both cases may be resolved by one or more reverting to backup and waiting unique amounts of time as recommended but this will not cover all failure modes.

T2-REC-0029: Chassis Managers **should** implement backup processes beyond those required here that are effective in all failure modes of any single component.

T2-REC-0031: Backup Chassis Managers **should** be chosen from those known or evidenced to be effective at working together in all of their failure modes.

T2-RUL-0311: Chassis Managers **shall** implement the defined messages in SECTION 5.3.3.3 when communicating on the MRI.

T2-REC-0032: Chassis Managers **should** implement additional messages to better record state, aid redundancy, and improve debugging.

5.3.3.3 Manager Redundancy Interface Protocol

This section contains definitions that specify the message structures and parameter values for the data sent or received over the MRI.

T2-REC-0033: The message structures used on the MRI **should** be transmitted as a byte aligned array with the following sections: $[Header][Payload][Trailer]$.

T2-RUL-0312: The MRI message header **shall** conform to the structure as specified in TABLE 5-8, TABLE 5-9, and TABLE 5-10.

Table 5-8 MRI message header structure

Index	Byte count	Description
0	2	Message ID
2	2	Data Type
4	2	Part of whole. Example: if message is x of y chunks, this parameter is x.
6	2	Whole. In the example above, this parameter would contain the value y.
8	2	Reserved. Unused, write as 0x0000.
10	2	Payload Length

Table 5-9 MRI message ID enumeration

Enumerated Type Name	Value
MRI_MESSAGE_ID_INVALID	0
MRI_MESSAGE_ID_HEARTBEAT	1
MRI_MESSAGE_ID_DATA_SYNC	2
MRI_MESSAGE_ID_CONFIGURATION	3
MRI_MESSAGE_ID_ACK	4
MRI_MESSAGE_ID_NACK	5

Table 5-10 MRI data type enumeration

Enumerated Type Name	Value
MRI_DATA_TYPE_INVALID	0
MRI_DATA_TYPE_FRU_RECORD	1
MRI_DATA_TYPE_SENSOR_DATA_RECORD	2
MRI_DATA_TYPE_PLATFORM_EVENT	3
MRI_DATA_TYPE_CHASSIS_ADDRESS_TABLE	4

Enumerated Type Name	Value
MRI_DATA_TYPE_CHASSIS_MANAGER_IP_RECORD	5
MRI_DATA_TYPE_RADIAL_SYSTEM_IPMB_LINK_MAP	6
MRI_DATA_TYPE_CHASSIS_FAN_GEOGRAPHY	7
MRI_DATA_TYPE_LED_DESCRIPTION	8
MRI_DATA_TYPE_CHASSIS_IPMB_DESCRIPTION	9

T2-RUL-0313: The message header parameter "Part of Whole" **shall** be used to represent the index of the data chunk in a sequence of related messages, same Message ID and Data Type. This index is used to assemble the entire message payload as one contiguous record on the receiving end point.

T2-RUL-0314: The MRI message payload for a heartbeat message **shall** conform the structure as specified in Table 5-11.

Table 5-11 MRI heartbeat payload structure

Index	Byte Count	Description
0	4	IP Address
4	1	Management State {UNABLE, BACKUP, ACTIVE}
5	1	IPMB Address
6	4	UTC Timestamp. 1 second resolution, unsigned.
10	4	(optional) High Resolution Offset. 1 micro second resolution, unsigned
14	4	Group IP Address.

T2-RUL-0315: The MRI message payload for the MRI_DATA_TYPE_FRU_RECORD data type **shall** conform to the structures defined in IPMI Version 2.0 Section 34.2.

T2-RUL-0316: The MRI message payload for the MRI_DATA_TYPE_SENSOR_DATA_RECORD data type **shall** conform to the structures defined in IPMI Version 2.0 Section 43.

T2-RUL-0317: The MRI message payload for the MRI_DATA_TYPE_PLATFORM_EVENT data type **shall** conform to the structure(s) defined in IPMI Version 2.0 Section 29.3.

T2-RUL-0318: The MRI message payload for the MRI_DATA_TYPE_CHASSIS_ADDRESS_TABLE data type **shall** conform to the structure defined in ANSI/VITA 46.11 Section 10.3.1.

T2-RUL-0319: The MRI message payload for the MRI_DATA_TYPE_CHASSIS_MANAGER_IP_RECORD data type **shall** conform to the structure defined in ANSI/VITA 46.11 Section 10.3.2.

T2-RUL-0321: The MRI message payload for the MRI_DATA_TYPE_RADIAL_SYSTEM_IPMB_LINK_MAP data type **shall** conform to the structure defined in ANSI/VITA 46.11 Section 10.3.3.

T2-RUL-0322: The MRI message payload for the MRI_DATA_TYPE_CHASSIS_FAN_GEOGRAPHY data type **shall** conform to the structure defined in ANSI/VITA 46.11 Section 10.3.4.

T2-RUL-0323: The MRI message payload for the MRI_DATA_TYPE_LED_DESCRIPTION data type **shall** conform to the structure defined in ANSI/VITA 46.11 Section 10.3.5.

T2-RUL-0324: The MRI message payload for the MRI_DATA_TYPE_CHASSIS_IPMB_DESCRIPTION data type **shall** conform to the structure defined in ANSI/VITA 46.11 Section 10.3.6.

T2-RUL-0325: The MRI message payload for the configuration data type **shall** conform to the structure as specified in Table 5-12.

Table 5-12 MRI configuration data structure definition

Index	Byte Count	Description
0	1	Min rate at which active Chassis Manager should be messaging (1-100) on the MRI
1	1	Min rate at which the active Chassis Manager should be messaging (1-100) on the IPMB
2	1	N number of messages that can be missed on the MRI before Chassis Manager with derived IPMB address of 82h can become active.
3	1	N number of messages that can be missed on the IPMB before Chassis Manager with derived IPMB address of 82h can become active.
…	…	…
32	1	N number of messages that can be missed on the MRI before Chassis Manager with derived IPMB address of 91h can become active.
33	1	N number of messages that can be missed on the IPMB before Chassis Manager with derived IPMB address of 91h can become active.

T2-RUL-0326: The MRI message payload for the NACK data type **shall** conform to the structure as specified in Table 5-13.

Table 5-13 MRI ACK and NACK message payload data structure definition

Index	Byte Count	Description
0	2	Reserved. Unused, write as 0x0000.
2	2	Error code (Table 5-14)

Table 5-14 MRI ACK and NACK payload error code enumeration

Enumerated Type Name	Value
MRI_ERROR_CODE_UNKNOWN	0
MRI_ERROR_CODE_SUCCESS	1
MRI_ERROR_CODE_UNSUPPORTED	2
MRI_ERROR_CODE_MESSAGE_ERROR	3
MRI_ERROR_CODE_RETRANSMIT	4

T2-RUL-0327: The MRI message trailer **shall** conform to the structure as specified in Table 5-15.

Table 5-15 MRI message trailer structure definition

Index	Byte Count	Description
0	2	Reserved. Unused, write as 0x0000.
2	2	CRC16-CCITT (polynomial 0x1021)

5.3.3.4 IPMCs

According to ANSI/VITA 46.11 an IPMC is,

> *The portion of a FRU that interfaces with a Chassis' IPMB and represents the FRU and any devices subsidiary to it. The IPMC is the lowest level physical management entity in the VPX System Management architecture. This term can apply either to the physical or logical entity which performs this function (depending on context).*

The following HOST requirements enable additional capabilities including access to the payload interface and ultimately to the System Manager, system modes, etc.

T2-RUL-0755: IPMCs **shall** utilize the system management buses SM[1..0] (IPMB-A) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-RUL-1106: IPMCs **shall** utilize the system management buses SM[3..2] (IPMB-B) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-OBS-0290: The SYSRESET* requirements of ANSI/VITA 46.11 Section 4.1.9 supersede the requirements of ANSI/VITA 65.0.

T2-OBS-0300: An IPMC may not be able to process a Command from a Chassis Manager if a fault has occurred on the HOST Module that is preventing an IPMC from processing and executing the Command. The IPMC could also be processing a previous Command and not have the ability to immediately respond to the Chassis Manager's Command.

T2-RUL-1945: IPMCs which are enabled for event generation **shall** send active event messages to the location indicated in the "Set Event Receiver" message when events are detected.

T2-OBS-0501: Per ANSI/VITA 46.11, the Set Event Receiver Message enables IPMCs to send Sensor Event messages upon the detection of a change in sensor status. These messages can therefore be sent based on the IPMC's determination of need, and not always in direct response to a Command from the Chassis Manager.

T2-RUL-0821: IPMCs **shall** implement, in either volatile or non-volatile memory, a System Event Log as defined in IPMI, Section 31 "System Event Log (SEL) Commands" and Section 32 "SEL Record Formats."

T2-RUL-0328: IPMCs **shall** be configurable to operate on IPMB-A from 100kHz to 400kHz.

T2-RUL-0329: IPMCs **shall** be configurable to operate on IPMB-B from 100kHz to 400kHz.

T2-REC-0052: IPMCs **should** have accessible methods for updating configuration parameters to allow for different system requirements.

5.3.3.5 HOST Messages

TABLE 5-16 represents IPMI formatted messages mandated by HOST. HOST standardizes interfaces including Chassis Manager-IPMB, IPMC-IPMB, IPMC-Payload Interface, Chassis Manager-Payload Interface, and the Chassis Manager-System Manager Interface. All other messages defined in ANSI/VITA 46.11 and IPMI are optional for this HOST standard.

T2-RUL-0331: Chassis Managers **shall use** unsigned 32-bit Coordinated Universal Time (UTC) time for all logged messages, data, and events.

T2-RUL-0332: Chassis Managers **shall** implement all the messages listed in TABLE 5-16 which are designated as mandatory for the Chassis Manager-IPMB interface.

T2-RUL-0333: Chassis Managers **shall** make all commands and data accessible through the System Manager Interface.

T2-RUL-0334: Chassis Managers **shall** make all commands and data accessible through the Payload Interface.

T2-RUL-0335: ChMCs for payload-resident Chassis Managers **shall** make all commands and data accessible through the Payload Interface.

T2-OBS-0071: This is consistent with ANSI/VITA 46.11 Rule 4.1.3-3, which requires a payload-resident Chassis Manager and ChMC utilize the Payload Interface for Rule 4.1.3-3's specified message set.

T2-RUL-0281: Chassis Managers **shall** have a Payload Interface accessible via test points.

T2-RUL-0282: ChMCs for payload-resident Chassis Managers **shall** have a Payload Interface accessible via test points.

T2-REC-0283: Integrators **should** provide the hardware specification for the Payload Interface chosen on Chassis Managers, ChMCs, and IPMCs in the HOST Tier 3 specification.

T2-RUL-0336: Chassis Managers **shall** implement only IPMI formatted messages.

T2-PER-0082: Chassis Managers **may** implement additional IPMI formatted messages than what is defined in TABLE 5-16.

T2-PER-0085: Chassis Managers **may** be exempted from transmitting messages based on superseding Platform requirements.

T2-OBS-0296: Superseding Platform requirements could include classified requirements, security guidelines, safety considerations, laws, regulations, or any other higher precedence requirements as defined by the program

T2-RUL-0337: IPMCs **shall** use unsigned 32-bit UTC time for all logged messages, data, and events.

T2-RUL-0338: IPMCs **shall** implement all the messages listed in TABLE 5-16 which are designated as mandatory for the IPMC-IPMB interface.

T2-RUL-0284: IPMCs **shall** make all commands and data accessible through the Payload Interface.

T2-RUL-0271: IPMCs **shall** have a Payload Interface accessible via test points.

T2-REC-0272: Integrators **should** provide the hardware specification for the Payload Interface chosen on Chassis Managers and IPMCs in the HOST Tier 3 specification.

T2-RUL-0339: IPMCs **shall** implement only IPMI formatted messages.

T2-PER-0083: IPMCs **may** implement additional IPMI formatted messages than what is defined in TABLE 5-16.

T2-OBS-0072: The rules of this section are requirements on hardware to include and support Hardware System Management messages, but it is left to the discretion of an integrator to determine when the use of a message is appropriate for each system. For example, an integrator can choose to utilize event generation or not.

T2-PER-0084: Payload Test Results Sensor Event Message Bytes 6 (Event Data 2) & 7 (Event Data 3) data **may** be used to provide additional supporting data.

T2-REC-0044: Integrators **should** provide all related information in regards to OEM (Original Equipment Manufacturer) defined information such as OEM codes to the applicable program management office for interoperability purposes.

Table 5-16 HOST Messages

Message Name	Standard section	IPMC - IPMB	CHMGR - IPMB
FRU Control	VITA 46.11, Section 10.1.3.6	M	AV 46.11 M
Set FRU State Policy BITs	VITA 46.11, Section 10.1.3.9	M	AV 46.11 M
Get FRU State Policy BITS	VITA 46.11, Section 10.1.3.8	M	AV 46.11 M
Get Mandatory Sensor Numbers	VITA 46.11, Section 10.1.3.26	M	M
Get SEL Info	IPMI V2.0, Section 31.2	M	AV 46.11 M
Get SEL Entry	IPMI V2.0, Section 31.5	M	AV 46.11 M
Get SEL Time	IPMI V2.0, Section 31.10	M	AV 46.11 M
Set SEL Time	IPMI V2.0, Section 31.11	M	AV 46.11 M
Set FRU Activation	VITA 46.11 Section 10.1.3.10	M	AV 46.11 M

Note: CHMGR = Chassis Manager

5.3.3.6 Mandatory HOST Sensors

The HOST Standard requires IPMCs and ChMCs to support additional sensors to the mandatory set of sensors called out in VITA 46.11.

T2-RUL-0341: IPMCs **shall** implement the FRU Mode Sensor for their FRU #0 with sensor number 7.

T2-PER-0058: A FRU Mode Sensor **may** be implemented by the IPMC for any Subsidiary FRU managed by that IPMC, using an IPMC-assigned sensor number.

T2-RUL-0342: A FRU Mode Sensor **shall** be implemented using Sensor Type F6h (HOST Mode) and event/reading code 6Fh (Sensor-specific).

T2-RUL-0343: IPMCs **shall** support the additional fields in TABLE 5-17 for the Response Data for the "Get Mandatory Sensor Numbers Command", See Table 10.1.3.26-1 in ANSI/VITA 46.11.

Table 5-17. Response Data for the "Get Mandatory Sensor Numbers" IPMI command

Byte	Data Field
9	FRU Mode Sensor Number (FFh if not supported for the FRU)

5.3.3.6.1 FRU Mode Sensor

This sensor tracks the current mode of an intelligent FRU as dictated by application software. It is defined for both intelligent and Subsidiary FRUs. The FRU Mode Sensor for an intelligent FRU (FRU #0) has a sensor number 7. FRU Mode Sensor for Subsidiary FRUs are assigned by the controlling IPMCs.

This sensor uses the Sensor Type value F6h. ANSI/VITA 46.11 Section 6.1 "Mandatory SDR Requirements" contains requirements related to the FRU Mode Sensor. The "Get Sensor Reading" command request and response format for this sensor is shown in TABLE 5-18.

Table 5-18 Get Sensor Reading (FRU Mode Sensor)

	Byte	Data Field
Request Data	1	Sensor Number
Response Data	1	Completion Code
	2	Sensor Reading [7:0] Not Used. Write as 00h, ignore on read
	3	Standard IPMI byte (See "Get Sensor Reading" in IPMI Specification): [7] – 0b = All Event Messages disabled from this sensor [6] – 0b = sensor scanning disabled [5] – 1b = reading/state unavailable (formerly "initial update in progress") [4:0] – reserved.
	4	Current Mode

	[7:4] – Reserved [3:0] – Current Mode 00h – Unknown Mode 01h – Operational Mode 02h – Maintenance Mode 03h – Debug Mode 04h – Load/Verify Mode 05h – Data Purge Mode 06h – Shut-Down Mode 07h – Failsafe Mode 08h-0Fh – User Defined Modes (Optional) 10h-FFh – Undefined
(5)	[7:0] – Optional/Reserved If provided, write as 80h (IPMI restriction). Ignore on read

The event message for this sensor has the format shown in TABLE 5-19 FRU Mode Sensor Event Message.

Table 5-19 FRU Mode Sensor Event Message

	Byte	Data Field
Request Data	1	Event Message Rev = 04h (IPMI 1.5)
	2	Sensor Type = F6h (FRU Mode sensor)
	3	Sensor Number
	4	[7] – Event Direction: 0b = Assertion, [6:0] – Event Type: 6Fh (Sensor-specific)
	5	Event Data 1 [7:4] – Ah (OEM code in Event Data 2, OEM code in Event Data 3) [3:0] – Current Mode: 00h – Unknown Mode

	01h – Operational Mode 02h – Maintenance Mode 03h – Debug Mode 04h – Load/Verify Mode 05h – Data Purge Mode 06h – Shut-Down Mode 07h – Failsafe Mode 08h-0Fh – User Defined Modes (Optional) 10h-FFh – Undefined
6	Event Data 2 [7:4] – Cause of Mode Change (see Table 5-20for values) [3:0] – Previous Mode: 00h – Unknown Mode 01h – Operational Mode 02h – Maintenance Mode 03h – Debug Mode 04h – Load/Verify Mode 05h – Data Purge Mode 06h – Shut-Down Mode 07h – Failsafe Mode 08h-0Fh – User Defined Modes (Optional) 10h-FFh – Undefined
7	Event Data 3 [7:0] – Payload Software Identifier.

Table 5-20 Cause of Mode Change Values", defines possible causes of FRU Operational Mode change.

Table 5-20 Cause of Mode Change Values

Value	Description
00h	Normal Mode Change. This is used when the payload software is normally proceeding through its modes.
01h	Software Exception. This is used when the payload software changed its mode in response to a software exception.
02h	User Initiated. This is used when the payload software changed its mode in response to a user initiated event.
03h	External Software. This is used when the payload software changed its mode in response to an external software application event (e.g. loader verifier application plugged in).
04h-0Fh	OEM defined.

5.4 Hardware

HOST standardizes hardware components so that each HOST Component, as defined in SECTION 5.4.2, can interface with another HOST Component. The different hardware components that are standardized are the Modules, Transmission Interfaces routed between Modules, and Enclosures. The HOST Components section contains the Form Factor and other mechanically oriented requirements for different hardware components, while the sections preceding it contain the electrically oriented requirements for different hardware components.

5.4.1 HOST Transmission Interfaces

The HOST Architecture establishes five Transmission Interfaces that facilitate logical and physical connectivity within the system. Each Transmission Interface, except for the SIOTI and *External I/O Transmission Interface* (EIOTI), contains elements of one or more planes defined in the ANSI/VITA 65.0 multi-plane architecture. This Tier 2 Core Technology Standard defines how the ANSI/VITA 65.0 multi-plane architecture is applied to the HOST Transmission Interfaces in 6U and 3U systems. These Interfaces are:

- **System Communications** - The SCTI utilizes the Data Plane, the UTP Control Plane, and the Expansion Plane.
- **Chassis Management** - The CMTI utilizes the ANSI/VITA 65.0 Utility Plane with the additional requirements of ANSI/VITA 46.11 for management communications. The ANSI/VITA 65.0 Control Plane may also be utilized for chassis management communications.
- **System I/O** - The SIOTI is an I/O routing layer that primarily utilizes the ANSI/VITA 65.0 User Defined I/O. The 6U Payload's 2 Thin-Pipes are also part of the SIOTI.
- **External I/O** - The EIOTI for this HOST Tier 2 Core Technology Standard includes the connectors used to bring the system I/O signals off the HOST Backplane, the connectors located on a front or rear panel, and any cables, connectors, and/or circuitry in between.

- **System Power Distribution** - The SPDI will use the power distribution portions of the ANSI/VITA 46.0 and ANSI/VITA 65.0 Utility Plane with input/output power interfaces as defined by ANSI/VITA 62.0 for modular power supplies and the requirements of the EIOTI contained in this document.

The HOST Tier 2 Transmission Interface configuration is shown in FIGURE 5.4-1.

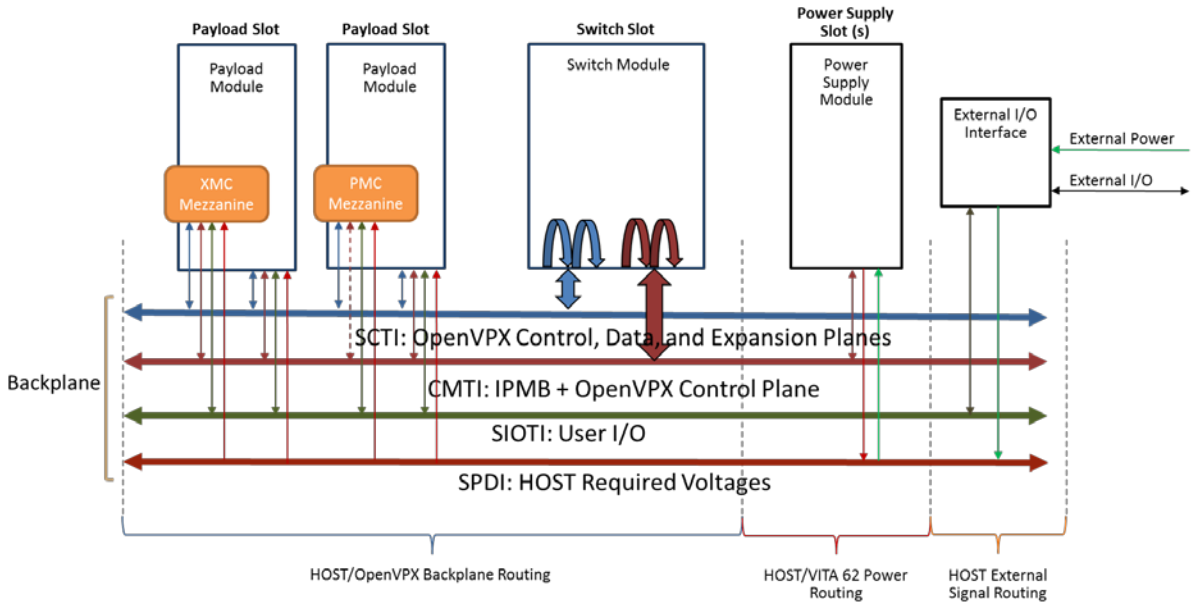

Figure 5.4-1 – HOST Tier 2 Transmission Interface Configuration

5.4.1.1 Common Transmission Interface Requirements

T2-RUL-2340: HOST Backplanes **shall** implement the requirements of ANSI/VITA 65.0, Section 7.2 through 7.4 (Common to 6U and 3U — *Backplane Profiles*).

T2-RUL-2390: Rear Transition Modules **shall** not be used to implement a Transmission Interface.

5.4.1.2 System Communications Transmission Interface Requirements

The HOST SCTI is implemented in hardware using OpenVPX switched fabric Backplane and PMC/XMC mezzanine technologies. The majority of requirements for SCTI implementations will come from the electrical and mechanical requirements of ANSI/VITA 65.0 (OpenVPX System Specification) for Backplanes. The SCTI functionality is performed by the OpenVPX Data Plane, Expansion Plane (for 6U only), and the UTP portion of the Control Plane high-speed serial interconnects. Functionality is extended to HOST Mezzanine Modules through PMC/XMC data bridges. The OpenVPX Data Plane transmits low-latency, high-bandwidth system data between modules utilizing Ethernet or PCI Express (PCIe). The OpenVPX Data Plane is typically a centralized switched network utilizing one or more switches. The switch, or switches, are classified as being part of the SCTI. The Expansion Plane protocol is PCIe and is typically used for communication between adjunct Modules and not through a Switch Module, though the HOST Standard does not limit the Expansion Plane to only be used in this manner. Mezzanine Module communications paths are also included as part of the SCTI. Mezzanine communications paths will sometimes include a bridge on the HOST Plug-In Module that translates PMC communications to the local bus of the Plug-In Module (usually PCI Express). In cases where resources

are co-located in hardware, the physical SCTI layers may be unneeded, leaving the SCTI logical communications to be performed completely within the hardware abstraction software layers.

5.4.1.2.1 Common System Communications Interface Requirements

T2-RUL-2930: The SCTI hardware components **shall** be defined as:

1. The Data Plane portion of an OpenVPX Backplane
2. The UTPs/Fat Pipes (FPs) of the Control Plane portion of an OpenVPX Backplane
3. OpenVPX conformant Plug-In network switches
4. The Expansion Plane portion of an OpenVPX Backplane

T2-OBS-0640: The SCTI is physically composed of an OpenVPX Backplane and Plug-In switch module(s) that perform the network packet switching.

T2-PER-0091: Although the Data Plane, Expansion Plane and Control Plane are separately labeled in a Slot Profile, Backplanes **may** connect interconnect ports labeled Data Plane, Control Plane, and Expansion Plane.

5.4.1.2.2 Mezzanine System Communications Interface Requirements

T2-RUL-2990: The SCTI **shall** include Payload Module's communications bridges to convert the SCTI protocols located on the Backplane to the appropriate PMC/XMC communications protocols for Mezzanine Modules.

T2-RUL-3000: If Payload Modules have HOST Mezzanine Module sites, SCTI communications bridges **shall** be located on the Payload Modules.

T2-PER-0180: Payload Modules that have attached mezzanines **may** be carrier boards where their only purpose is to support Mezzanine Modules.

T2-RUL-3010: The SCTI, as bridged to mezzanine slots, **shall** conform to the communications requirements of one of the following mezzanine card standards:

1. IEEE Std. 1386.1 Standard for PCI Mezzanine Cards
2. ANSI/VITA 42 Standards for Switched Mezzanine Cards

T2-RUL-3020: Requirements for SCTI mezzanine communications **shall** be applied using the following order of precedence:

1. Requirements of this Tier 2 HOST Standard (including additions or exclusions to PMC/XMC standards).
2. Mezzanine Module requirements of IEEE 1386.1 and ANSI/VITA 42.0 for PMCs and XMCs respectively.

T2-RUL-3030: The SCTI as bridged to PMC Mezzanine Modules **shall** conform to PMC 64-bit 33/66MHz PCI V2.3 communications standard.

T2-RUL-3040: The SCTI as bridged to XMC Mezzanine Modules **shall** conform to ANSI/VITA 42.3, American National Standard for XMC PCI Express Protocol Layer Standard.

T2-OBS-0650: XMC Mezzanine Modules that conform to parallel and Serial RapidIO protocols are not permitted in this standard.

5.4.1.3 System I/O Transmission Interface Requirements

The SIOTI is implemented as internal routing on the OpenVPX Backplane and connects the EIOTI with the User Defined and Thin-Pipe Ethernet pins of the HOST Plug-In Module slots. The SIOTI is intended for routing external I/O to and from modules and cannot be used for custom, inter-module communications that circumvent the chassis management, modularity, and openness of HOST.

5.4.1.3.1 Common System I/O Interface Requirements

T2-RUL-3050: The SIOTI hardware components **shall** be implemented as internal routing on the OpenVPX Backplane.

T2-PER-0185: Optical Signals **may** be implemented over an optical fiber cable going directly from the Platform to a Module Slot containing an ANSI/VITA 66.0 compliant connector.

T2-RUL-3080: All user defined pins, as defined in the HOST Module Slot Profiles **shall** be transmitted exclusively via the SIOTI.

T2-OBS-0660: The SIOTI connector pinouts with respect to mezzanine interfaces are referenced in SECTION 5.1.1.1.2.2 AND SECTION 5.1.1.1.3.6.

5.4.1.3.2 Backplane System I/O Interface Requirements

T2-RUL-3090: The SIOTI Backplane routing **shall** provide connectivity between the SIOTI and the EIOTI.

T2-OBS-0670: The user defined signals transmitted by the SIOTI are generically defined by the Slot and Module Profiles.

5.4.1.4 External I/O Transmission Interface Requirements

This Tier 2 HOST Standard broadly defines the Backplane mechanical and electrical connector interface portions of the EIOTI giving it the flexibility to meet the mechanical and electrical constraints of a Target System. This Tier 2 HOST Standard does not define the Target System interface panel mechanical and electrical portions of the EIOTI as that is defined by the Target System requirements.

The EIOTI Interconnect Diagram is shown in FIGURE 5.4-2.

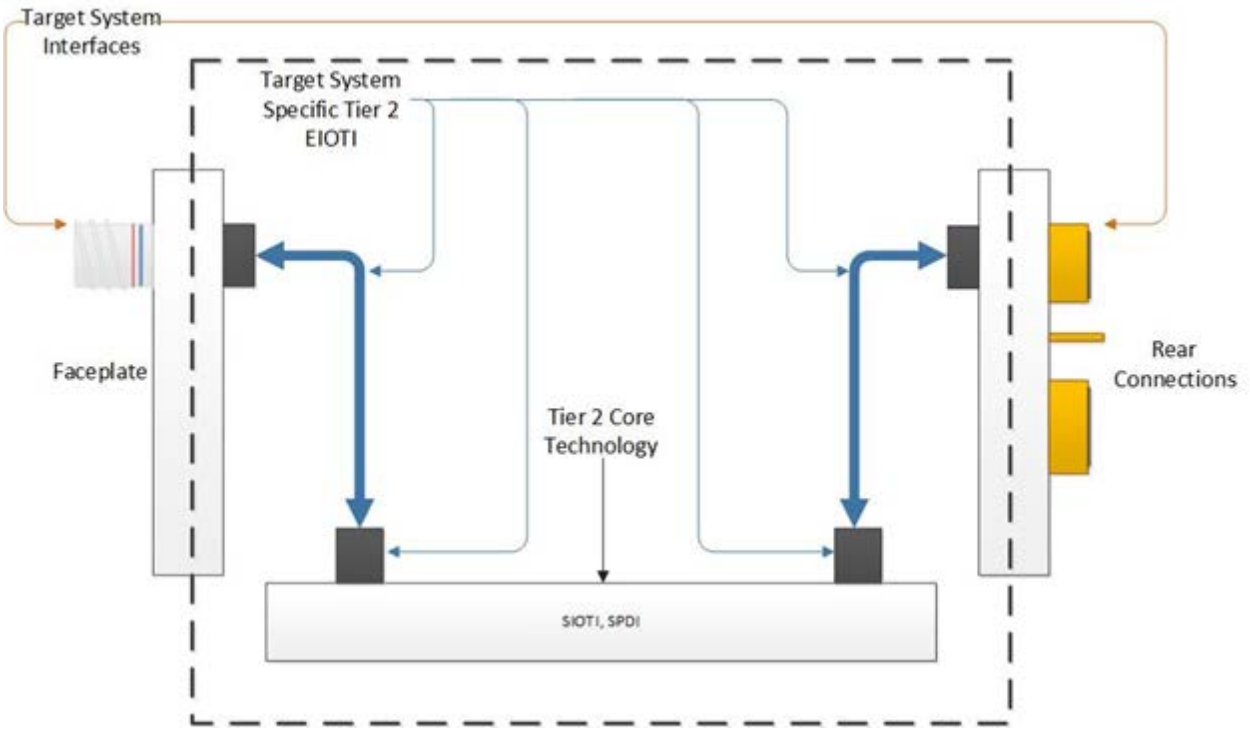

Figure 5.4-2 – HOST EIOTI Interconnect Diagram

T2-REC-0035: The EIOTI **should** be a modular unit that can be disconnected from the OpenVPX Backplane.

T2-OBS-0680: Modular EIOTI units facilitate HOST implementation migration and Target System lifecycle upgradeability and serviceability requirements.

T2-RUL-3120: The EIOTI **shall** provide connectivity between the external I/O at an Enclosure-level panel interface and the SIOTI at a Backplane interface.

T2-RUL-3130: The EIOTI **shall** provide connectivity between the Target System input power at an Enclosure-level panel interface and the SPDI at a Backplane interface.

T2-OBS-0690: The mechanical requirements for EIOTI modules are addressed in SECTION 5.4.2.

T2-RUL-3140: All external panel I/O signals **shall** pass through the EIOTI Backplane connector(s) before going to any HOST Module.

T2-PER-0195: The ANSI/VITA 66 and 67 family of blind mate connectors **may** be considered an EIOTI Backplane connector.

T2-OBS-0700: External front or rear panel chassis I/O signals include video and power.

T2-RUL-3150: All SIOTI Interface signals **shall** pass through the EIOTI Backplane connector(s) before going to any external front or rear panel chassis I/O connectors.

T2-OBS-0705: When connecting the front/rear panel connectors directly to the Backplane, those connectors are considered the EIOTI Backplane connectors.

T2-RUL-3170: All EIOTI Backplane connectors **shall** be commercially available connectors that can be procured by any vendor without prior authorization from any source (e.g. a commercial part governed by a source control drawing).

T2-RUL-3180: The EIOTI **shall** provide a path for connecting chassis ground to the SPDI at the HOST Backplane in support of ANSI/VITA 65.0, Section 3.2.3, Safety Ground.

5.4.1.5 Chassis Management Transmission Interface Requirements

The CMTI is implemented in hardware using OpenVPX Backplane technology. The majority of requirements for CMTI implementations will come from the electrical and mechanical requirements of ANSI/VITA 65.0 (OpenVPX System Specification) for Backplanes. CMTI functionality is performed by portions of the OpenVPX Control Plane, the OpenVPX Utility Plane and the OpenVPX Management Plane implementing ANSI/VITA 46.11. The OpenVPX Control Plane may be used for transmission of messages and large data transfers such as *Operational Flight Program* (OFP) loading. The OpenVPX Utility Plane includes power distribution functions and common control/status signals. The CMTI only includes the control/status functions of the OpenVPX Utility Plane. The OpenVPX Management Plane is implemented using the IPMB, where the Backplane contains the physical bus portion of the IPMB and Plug-In Modules contain an IPMC.

5.4.1.5.1 Common Chassis Management Transmission Interface Requirements

T2-RUL-3190: The CMTI hardware components **shall** be implemented utilizing:

1. The Backplane-routed control and status portions of the OpenVPX Utility Plane
2. The IPMB OpenVPX Management Plane
3. The UTP Control Plane Ethernet

T2-RUL-3270: HOST Backplanes **shall** implement a single, 2.49K Ohm, +/- 1%, pull-up resistor from each CMTI IPMB signal to the 3.3V Auxiliary voltage rail.

T2-OBS-0750: The single pull-up resistor supersedes ANSI/VITA 46.0 Rule 7-1, requiring spare resistors for both single-ended and differential termination schemes.

T2-RUL-3280: HOST Modules **shall** have zero pull-up resistors on the CMTI IPMB signals.

T2-OBS-0760: The rule against HOST Modules having pull-up resistors on the IPMB is a clarification of ANSI/VITA 46.11 Rule 9.2.3-2.

T2-RUL-3290: HOST Modules containing resources to drive the Utility Plane REF_CLK+/- signals **shall** provide a mechanism to permit *Application Software* or system management to reassign the identity of the SYS_CON module, regardless of the logic level of the Backplane SYS_CON* contact, in order to control these signal drivers once the Backplane power rails are all at minimum operating voltages as defined in ANSI/VITA 46.0, Section 4.8.12.4.

T2-OBS-0765: The SYS_CON module identity reassignment is a Recommendation 3.4.1-1 in ANSI/VITA 65.0.

T2-RUL-3291: The NVMRO portion of the CMTI **shall** conform to the low current open-drain signal specifications of ANSI/VITA 65.0, Section 3.3.1.

T2-RUL-3300: The SYSRESET* portion of the CMTI **shall** conform to the high current open-drain signal specifications of ANSI/VITA 65.0, Section 3.3.3 (High Current Open-Drain).

T2-RUL-3310: HOST Plug-In Modules receiving SYSRESET* as an input **shall** be able to register a valid low for any pulse length of 10ms or longer.

T2-RUL-3320: Payload Modules **shall** make SYSRESET* available to any HOST Mezzanine Module connector that has SM1 and SM0 available per ANSI/VITA 65.0 Recommendation 3.4.2.1-1.

T2-RUL-3321: The Backplane **shall** provide a method for optionally pulling the SYS_CON* signal low for all Payload and Switch Slots.

T2-RUL-3322: GAP* and GA[4:0] **shall** be wired to indicate physical slot numbers, with the numbers going from 1 thru N, where N is the number of slots.

T2-RUL-3330: HOST Plug-In Modules **shall** receive a unique Site Number that is based upon the Module's ANSI/VITA 65.0, Section 3.4.6, Geographic Address.

T2-OBS-0770: ANSI/VITA 65.0, Section 3.4.6, Geographic Address Field, specifies how geographical addressing is accomplished for OpenVPX modules.

T2-OBS-0775: It is recommended in ANSI/VITA 46.0 that *Joint Test Action Group* (JTAG) pins not be bussed on Backplanes.

T2-OBS-0790: ANSI/VITA 65.0, Section 3.4.7, JTAG Port, specifies that each P0/J0 connector must support the JTAG signal assignment established in ANSI/VITA 46.0. The JTAG port is designated for single-card use outside of the Target System only. For example, it can be used for single-card manufacturing, programming, or debug purposes.

T2-RUL-3370: The Control Plane as defined in SECTION 5.1.1.1 and SECTION 5.1.1.3 **shall** be included as part of the CMTI.

T2-RUL-3371: If a Payload Module has an XMC Mezzanine site, the Payload Module **shall** route the ANSI/VITA 42.0 defined I2C connections from the XMC Mezzanine Site to the IPMC of the Payload Module.

T2-OBS-0792: XMC Mezzanine Modules conform to the requirements for supporting the CMTI through the IPMC located on the parent Payload Modules. An example is illustrated in FIGURE 5.4-3.

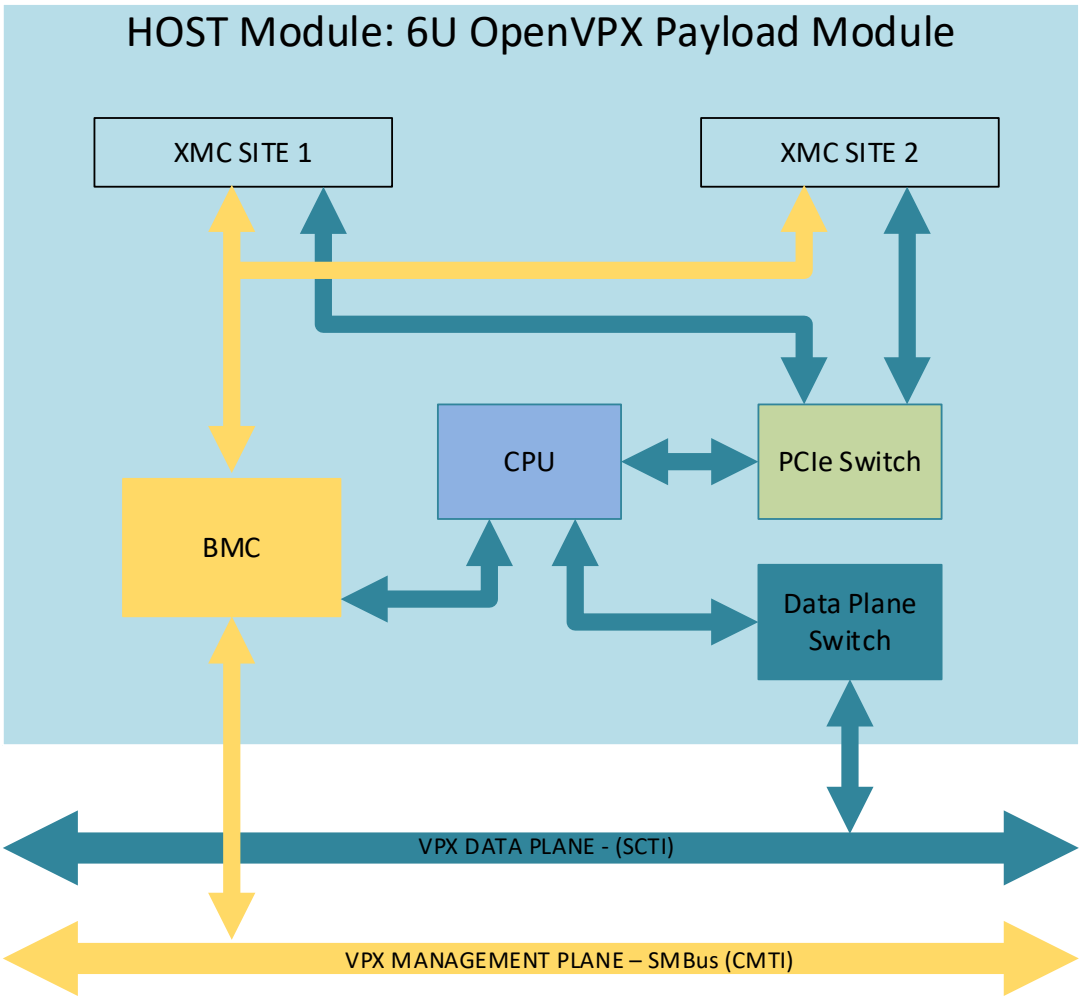

Figure 5.4-3 – Example HOST Payload Module XMC Mezzanine CMTI Configuration

T2-OBS-0793: PMC Mezzanine Modules conform to the requirements for supporting the CMTI through the parent Payload Module utilizing software components. An example is illustrated in FIGURE 5.4-4.

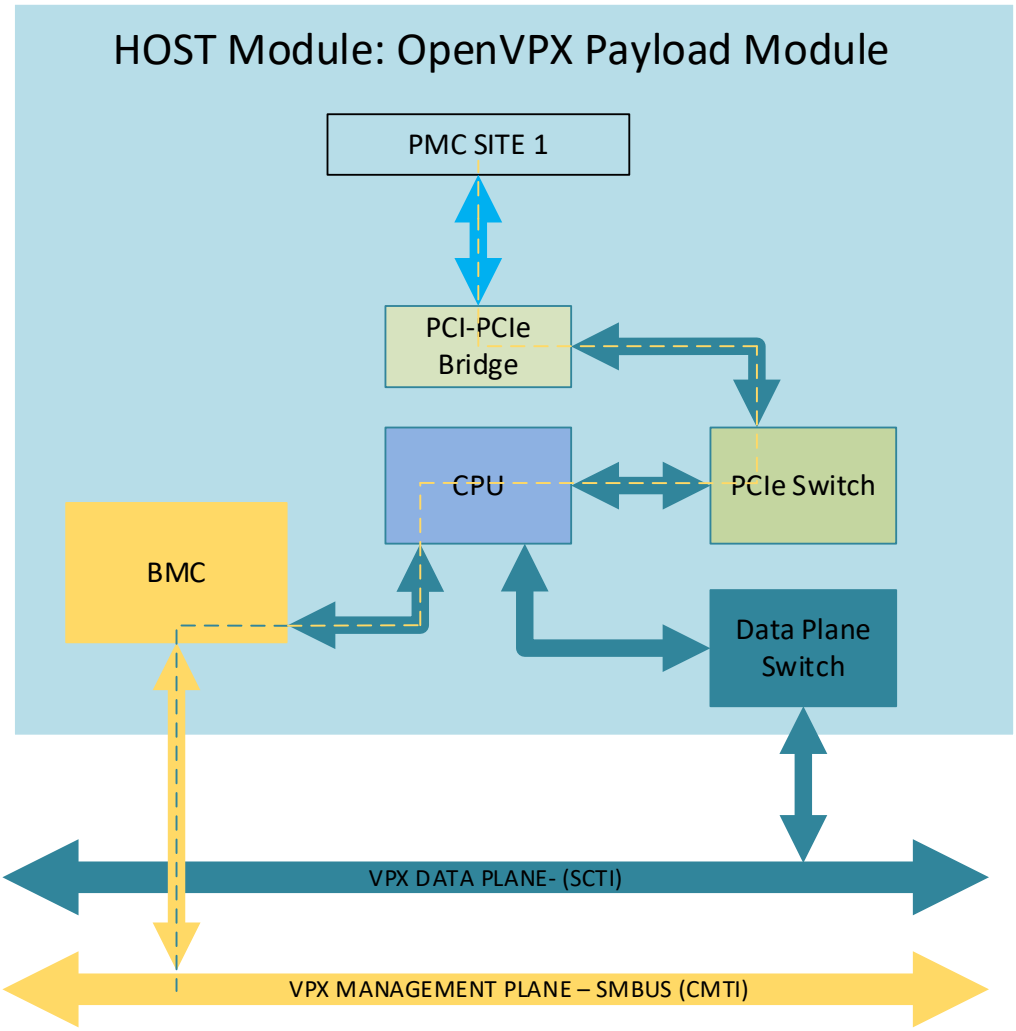

Figure 5.4-4 – Example HOST Payload Module PMC Mezzanine CMTI Configuration

5.4.1.5.2 6U Chassis Management Interface Requirements

T2-RUL-3220: The 6U hardware components implementing the IPMB Management Plane **shall** conform to the electrical requirements of ANSI/VITA 46.11 as applied to 6U OpenVPX implementations except where specified herein.

T2-RUL-3250: The 6U CMTI electrical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 6U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-RUL-3260: The 6U CMTI mechanical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 6U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-OBS-0710: HOST power distribution is accomplished with the SPDI.

T2-OBS-0730: ANSI/VITA 65.0, Section 3.3, Electrical Standards for Drivers and Receivers, specifies the electrical parameters for the OpenVPX Utility Plane.

T2-OBS-0740: ANSI/VITA 65.0, Section 3.4, System Control Signals, defines the OpenVPX Utility Plane signals and their functionality.

5.4.1.5.3 3U Chassis Management Interface Requirements

T2-RUL-3261: The 3U hardware components implementing the IPMB Management Plane **shall** conform to the electrical requirements of ANSI/VITA 46.11 as applied to 3U OpenVPX implementations except where specified herein.

T2-RUL-3262: The 3U CMTI electrical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 3U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-OBS-0741: HOST power distribution is accomplished with the SPDI.

T2-OBS-0742: ANSI/VITA 65.0, Section 3.3, Electrical Standards for Drivers and Receivers, specifies the electrical parameters for the OpenVPX Utility Plane.

T2-OBS-0743: ANSI/VITA 65.0, Section 3.4, System Control Signals, defines the OpenVPX Utility Plane signals and their functionality.

T2-OBS-0744: 3U Power Supply Modules only have GA[1:0] due to pin count. If it is desired that the PSM be higher than slot 4, offset logic will need to be implemented. For example, a specific Backplane power supply start at logical slot 6, for 3U PSMs GA1 GND and GA0 Open would mean logical slot 7.

5.4.1.6 System Power Distribution Interface Requirements

The HOST SPDI primary function is distributing power to Plug-In Modules. The SPDI distributes defined voltages to each payload and switch slot on the HOST Backplane via the OpenVPX Utility Plane. The ANSI\VITA 65.0, signals VS1, VS2, VS3, 3.3V_AUX, and +/-12V_AUX of the OpenVPX Utility Plane make up the SPDI. The SPDI is also responsible for transporting prime power to the *Power Supply Resource* (PSR) and intermediate power between PSR stages and/or to Energy Storage Modules described in SECTION 5.1.1.2.

5.4.1.6.1 Common System Power Distribution Interface Requirements

T2-RUL-3420: The SPDI **shall** conform to the Backplane requirements of ANSI/VITA 65.0, Section 3.2 except where specified herein.

T2-RUL-3430: For HOST Payload and Switch Slots the SPDI **shall** exclusively support the Power Distribution portion of the OpenVPX Utility Plane.

T2-RUL-2360: HOST Backplanes **shall** size Vs1 to be able to distribute at least 14 A per slot. Refer to connector current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-RUL-2365: HOST Backplanes **shall** size Vs2 to be able to distribute at least 14A per slot. Refer to connector current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-RUL-2375: HOST Backplanes **shall** have a 4.7K pull-up on the PSM slot's FAIL* signal, as is recommended in Observation 4.6.3.7-1 of ANSI/VITA 62.0.

T2-RUL-3460: If a Payload Module supports a PMC site, a Payload Module **shall** route the SPDI to the appropriate PMC connectors per IEEE 1386.1.

T2-RUL-3465: If a Payload Module supports a XMC site, a Payload Module **shall** route the SPDI to the appropriate XMC connectors per ANSI/VITA 42.0.

T2-OBS-0820: Due to the site profile provided for PMCs, a Payload Module implementing that site profile will need to route the SPDI to both the XMC and PMC connectors.

T2-RUL-3470: The SPDI **shall** conform to the requirements for Single-Stage or Two-Stage power subsystems as specified by ANSI/VITA 62.0.

T2-OBS-0830: If a subsystem requires any Energy Storage Modules then the SPDI also must support the Energy Storage Module.

T2-RUL-3480: The SPDI **shall** provide a Backplane interface connector for transmitting Platform power from the EIOTI to the SPDI.

T2-RUL-3490: The SPDI **shall** receive a chassis ground signal from the EIOTI.

5.4.1.6.2 6U System Power Distribution Interface Requirements

T2-RUL-3491: The SPDI for 6U systems **shall** conform to the 12V High Voltage Power Input requirements of ANSI/VITA 46.0, section 4.8.1.1.3.

T2-RUL-3400: The SPDI for 6U component interfaces **shall** conform to the 6U Backplane electrical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-RUL-3410: The SPDI for 6U component interfaces **shall** conform to the 6U Backplane mechanical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-OBS-0810: Some sections of ANSI/VITA 62.0 and 65.0 contain requirements for air-cooled modules only. These requirements are not applicable to this Tier 2 technology.

T2-RUL-2370: HOST Backplanes **shall** size Vs3 to be able to distribute at least 22 A per 6U slot. Refer to current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-OBS-0811: The power rail sizes are the recommended minimums from ANSI/VITA 65.0, Section 11.2.1.2.1.

5.4.1.6.3 3U System Power Distribution Interface Requirements

T2-RUL-2374: The SPDI for 3U system **shall** conform to the High Voltage Power Input requirements of ANSI/VITA 46.0, Section 4.8.1.1.4.

T2-RUL-2371: The SPDI for 3U component interfaces **shall** conform to the 3U Backplane electrical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-RUL-2372: The SPDI for 3U component interfaces **shall** conform to the 3U Backplane mechanical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-OBS-0812: Some sections of ANSI/VITA 62.0 and 65.0 contain requirements for air-cooled modules only. These requirements are not applicable to this Tier 2 technology.

T2-RUL-2373: HOST Backplanes **shall** size Vs3 to be able to distribute at least 15 A per 3U slot. Refer to current load limits in ANSI/VITA 46.0, section 4.8.1.

T2-OBS-0813: The power rail sizes are the recommended minimums from ANSI/VITA 65.0 Section 15.2.1.2.1.

5.4.2 HOST Components

A notional layout for a HOST implementation is presented in FIGURE 5.4-5. This figure shows a hypothetical design to provide clarification for HOST Component descriptions. Layouts for specific Enclosure designs will vary.

As seen in the figure, the system for this Tier 2 technology comprises components from four categories, defined in the following sections:

- **HOST Enclosure –** The Enclosure design is variable and is designed to suit the requirements of the Target System. In the following notional views, it is approximated by a standard 1 ATR Enclosure, defined in ARINC 404A.
- **HOST Module –**Payload Module, Switch Module, PMC/XMC Mezzanine Module, or Power Supply Module.
- **HOST Backplane –** A physical circuit card assembly that accepts HOST Plug-In Modules and provides access to HOST Transmission Interfaces. The transmission components may also consist of discrete wires or cable assemblies serving as the connection between HOST Modules and *HOST External Interfaces*.
- **HOST External Interfaces –** External interfaces transfer signals and power between the HOST Transmission Components and the external system.

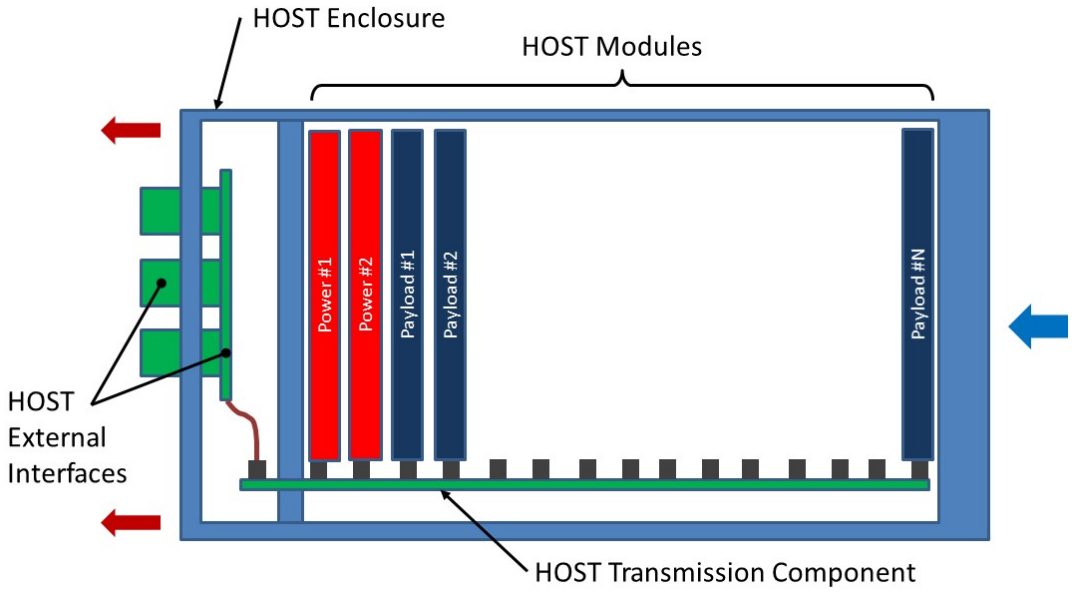

Figure 5.4-5 – Notional Side View of a Generic ATR Mission Computer

T2-RUL-3510: Environmental and performance tests, where applicable, **shall** be done in accordance with ANSI/VITA 47 per TABLE 5-21.

Table 5-21 Environmental and Performance Test Requirements

Environment	ANSI/VITA 47 Section
Operating Temperature	4.1
Non-Operating Temperature	4.2
Temperature Cycling	4.3
Vibration	4.4
Shock	4.5
Humidity	4.6
Altitude	4.7
Rapid Decompression	4.8
Attitude	4.9
Fungus Resistance	4.10
Electrostatic Discharge Resistance (With Optional Covers)	4.11
Corrosion Resistance	4.12

5.4.2.1 HOST Enclosure

5.4.2.1.1 Form Factor

T2-OBS-0840: External form factor requirements will be dictated by the requirements of the Target System.

T2-RUL-3520: The Payload Module region of the HOST Enclosure **shall** house Payload Modules as defined by SECTION 5.1.1.1.

T2-RUL-3530: The Switch Module region of the HOST Enclosure **shall** house Switch Modules as defined by SECTION 5.1.1.3.

T2-RUL-3540: The Power Supply Module region of the HOST Enclosure **shall** house power supply modules as defined in SECTION 5.1.1.2.

5.4.2.1.2 Card Cage Environment and Form Factor

T2-RUL-3550: The HOST Enclosure **shall** have rail geometry in accordance with IEEE 1101.2-1992 (R2008). Note: IEEE-1101.2-1992 (R2008) uses the term “Card Guide Slots” instead of “Rails”.

T2-RUL-3560: The card cage rail **shall** have a pitch of 1 inch for all electronic module slots.

T2-OBS-0850: The rail geometry for 6U is further specified in FIGURE 5.4-6 and the rail geometry for 3U is further specified in FIGURE 5.4-7.

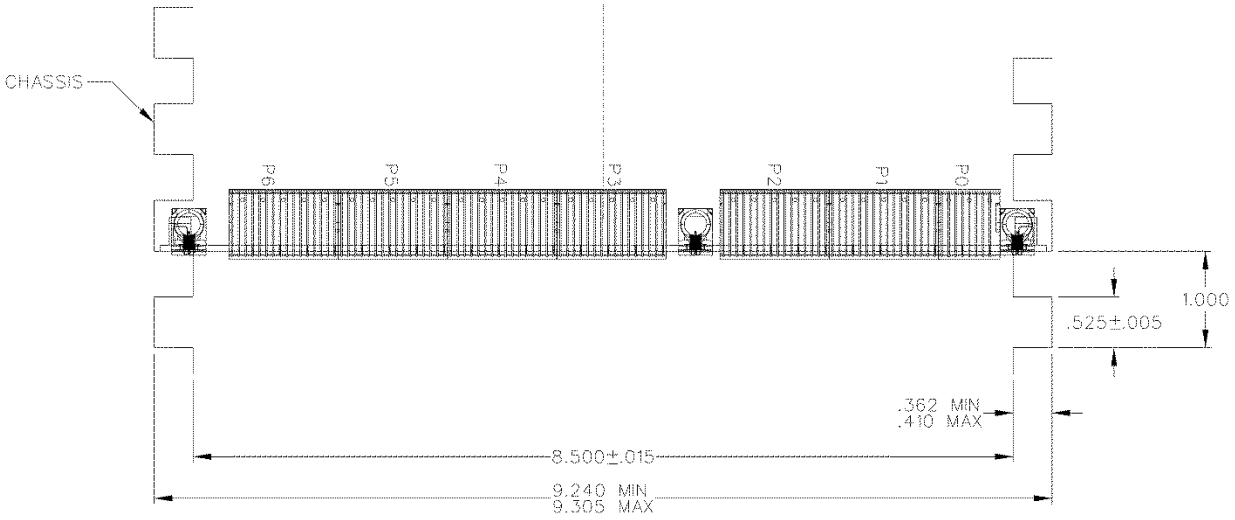

Figure 5.4-6 – 6U Rail Geometry

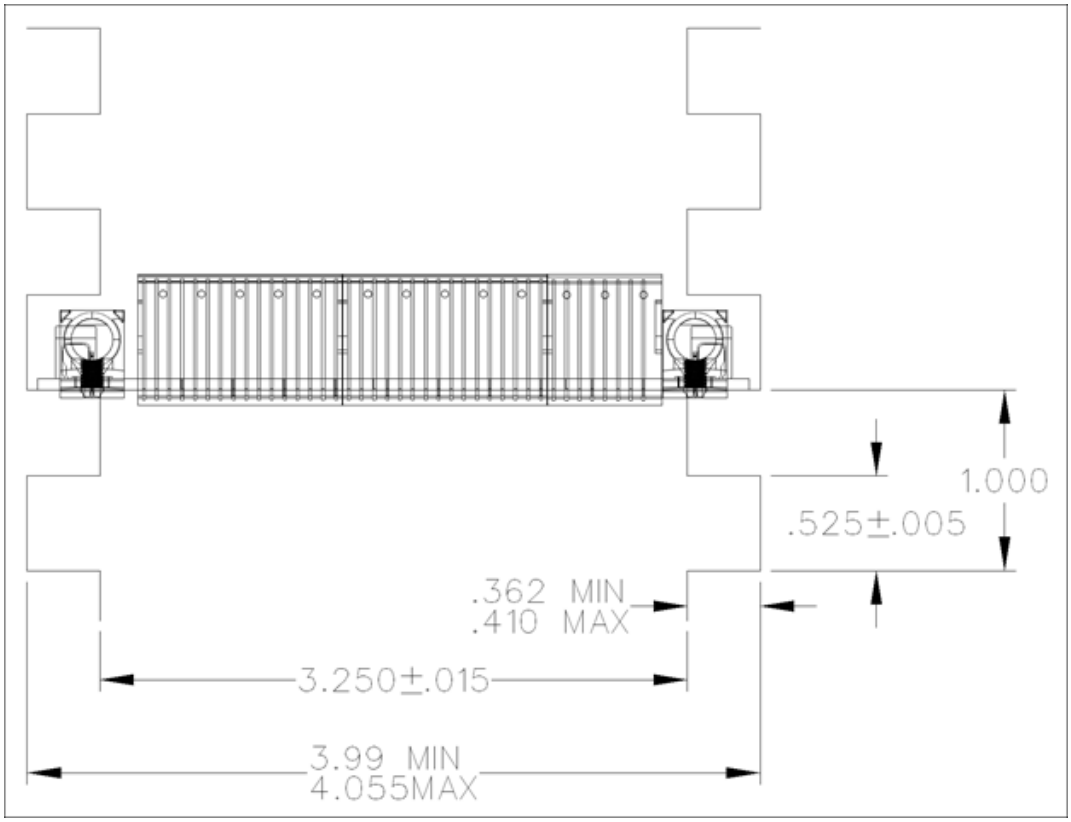

Figure 5.4-7 – 3U Rail Geometry

T2-RUL-3570: The card cage **shall** utilize wedgelocks as defined in ANSI/VITA 46.0, Appendix A.

T2-RUL-3580: The HOST Enclosure card cage **shall** provide conduction cooling to the electronic modules.

T2-RUL-3590: The HOST Enclosure card cage **shall** provide a module rail temperature less than or equal to +85°C during the worst-case thermal loading with all slots filled unless otherwise specified by the Target System.

T2-OBS-0851: T2-RUL- 3590 specifies the maximum temperature on the Plug-In Module side of the thermal interface between Plug-In Modules and chassis. The temperature gradient between the Plug-In Module edge and the chassis can be an issue in systems that are not properly designed.

5.4.2.2 HOST Module

The standards of this section define the module requirements for the Tier 2 Standard.

5.4.2.2.1 Form Factor

The form factor for standard HOST OpenVPX Payload and Switch Modules is defined in ANSI/VITA 65.0, Section 4. ANSI/VITA 65.0 passes the majority of these requirements through from ANSI/VITA 46.0 and ANSI/VITA 48 dot standards, which refer to standard form factors defined in IEEE 1101.1 and IEEE 1101.2. HOST recommends following ANSI/VITA 48.2, IEEE 1101.1, and IEEE 1101.2 for guidance regarding form factor of HOST 6U and 3U Modules.

T2-RUL-3610: Payload Modules **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 65.0 for conduction cooled modules
3. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

T2-RUL-3620: Switch Modules **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 65.0 for conduction cooled modules
3. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

T2-RUL-3630: PMC Mezzanine Modules **shall** adhere to form factor constraints provided in IEEE 1386.

T2-RUL-3631: XMC Mezzanine Modules **shall** adhere to form factor constraints provided in ANSI/VITA 42.0.

T2-RUL-3640: HOST Mezzanine Modules **shall** pass qualification testing while installed on the Payload Module including all hardware and accessories.

T2-OBS-0870: HOST Mezzanine Modules **may** undergo preliminary testing, but it is a higher priority to characterize the effect of Mezzanine Modules on other resources.

5.4.2.2.2 Interfaces

T2-RUL-3670: HOST Plug-In Modules **shall** use alignment-keying sockets defined in ANSI/VITA 46.0, Table 4-2.

T2-RUL-3680: HOST Plug-In Modules **shall** use alignment keys as defined in ANSI/VITA 46.0, Section 4.4.3 Plug-In Module Key.

T2-PER-0011: HOST Plug-In Modules **may** use the Ruggedized Machined 6061 Aluminum RT2-R compatible keying guide sockets.

T2-OBS-0880: The actual keying positions of the Plug-In Modules will depend on the orientation of the keying pins of the HOST Backplane slot the baseboard is interfacing with.

T2-REC-0045: With higher shock and vibration environments, Payload and Switch Modules **should** use the 3700, or equivalent.

T2-REC-0046: Alignment pin keying information for Plug-In Modules **should** be documented.

T2-RUL-3720: HOST Plug-In Modules **shall** prohibit features that prevent installation in a HOST Enclosure.

T2-RUL-3730: No additional components **shall** be required to install a Plug-In Module in a HOST Enclosure other than those typically used for ANSI/VITA compliant OpenVPX modules.

5.4.2.2.2.1 6U Interfaces

T2-RUL-3690: 6U Power Supply Modules **shall** follow the rules defined in ANSI/VITA 62.0, Section 4.3.2 6U Slot Keying and in Section 6.3 Alignment and Keying.

T2-RUL-3700: 6U Payload Modules **shall** use connectors defined in ANSI/VITA 46.0, Table 6-1, or the rugged equivalent RT2-R, unless following SECTION 5.1.1.1.2.3.

T2-PER-0205: 6U Payload Modules **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.2.3.

5.4.2.2.2.2 3U Interfaces

T2-RUL-3701: 3U Power Supply Modules **shall** follow the rules defined in ANSI/VITA 62.0, Section 4.3.1 3U Slot Keying and in Section 5.3 Alignment and Keying.

T2-RUL-3702: 3U Payload Modules **shall** use connectors defined in ANSI/VITA 46.0, Table 5-1, or the rugged equivalent RT2-R, unless following SECTION 5.1.1.1.3.7.

T2-PER-0206: 3U Payload Modules **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.3.7.

5.4.2.2.3 Environmental Requirements

T2-RUL-3741: HOST Modules **shall** perform to one, or more, of the classes called out in ANSI/VITA 47.

T2-RUL-3770: HOST Modules that perform in environments not included in the ANSI/VITA 47 standard **shall** provide information on acceptable environmental conditions.

T2-RUL-3780: Conformal coating for HOST Modules **shall** be applied per IPC J-STD-001F.

T2-RUL-3790: Materials used for conformal coating **shall** conform to IPC-CC-830B and be included in QPDSIS-46058.

5.4.2.3 HOST Transmission Components

HOST Transmission Components facilitate physical connectivity of power and communications signals between HOST Modules. The standard transmission component for OpenVPX is a Backplane that interfaces with standard Plug-In Modules. This standard defines the required form factor, interfaces, environmental requirements, and documentation requirements for the HOST OpenVPX Backplane.

5.4.2.3.1 Form Factor

The form factor for standard HOST OpenVPX Backplane is defined in ANSI/VITA 65.0, Section 4. ANSI/VITA 65.0 essentially passes these requirements through from ANSI/VITA 46, which refer to standard form factors defined in IEEE 1101.1 and IEEE 1101.2. FIGURE 5.4-8 shows the required 6U slot form factor derived from these standards and FIGURE 5.4-9 shows the required 3U slot form factor.

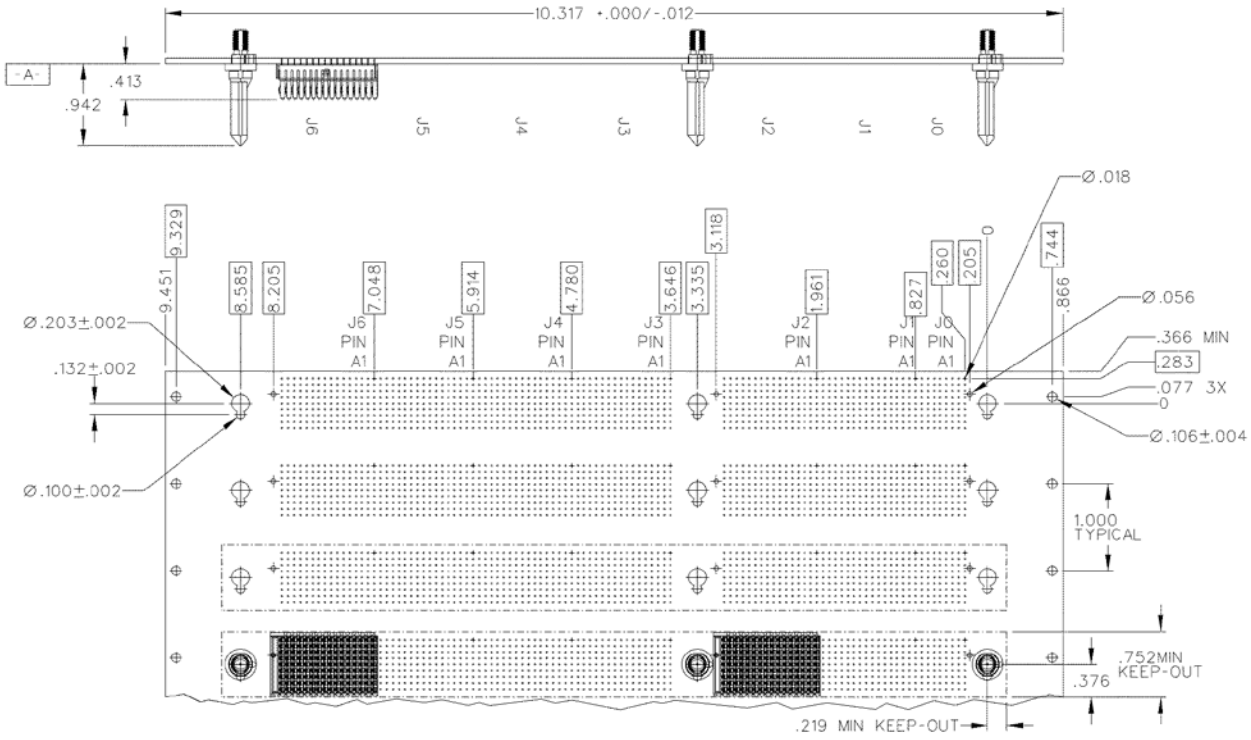

Figure 5.4-8 – 6U OpenVPX Backplane Form Factor

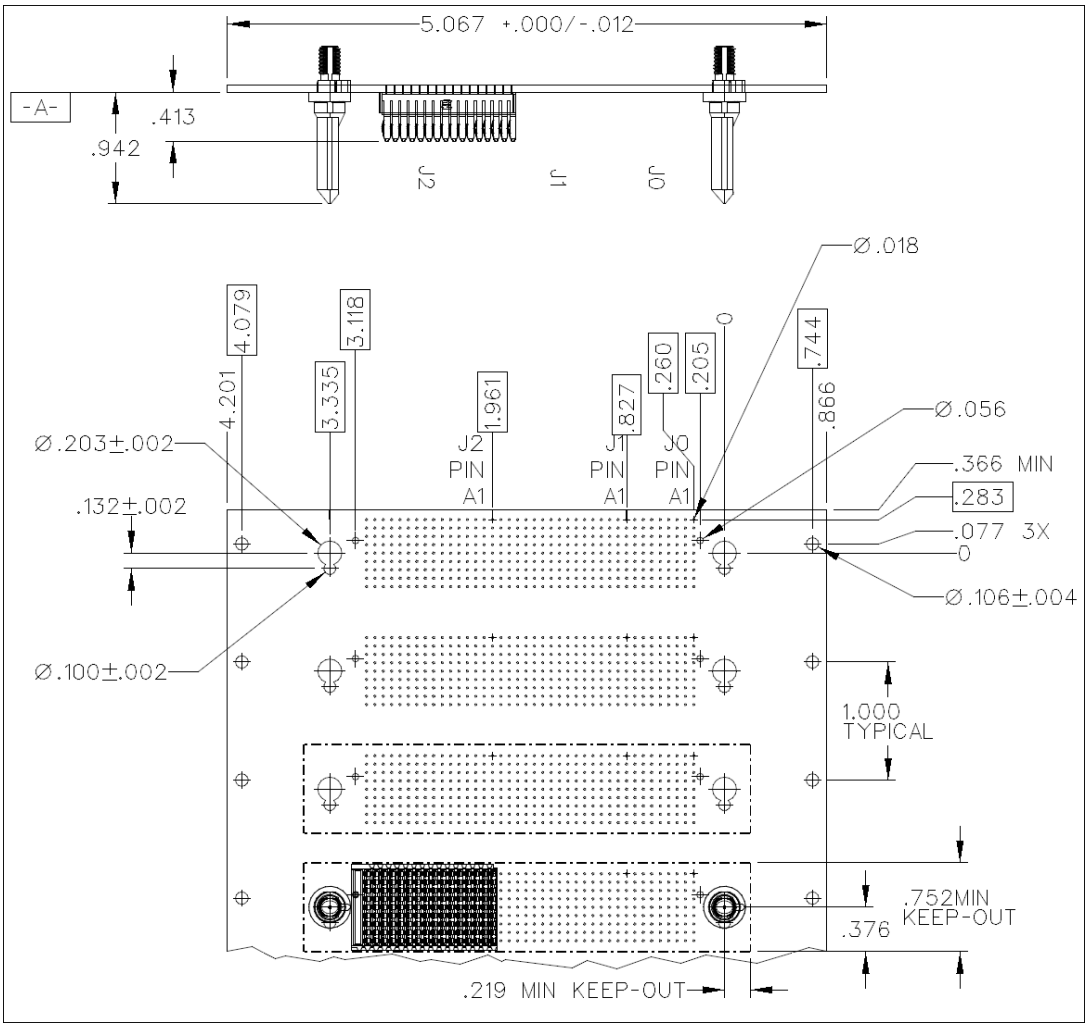

Figure 5.4-9 – 3U OpenVPX Backplane Form Factor

T2-OBS-0900: FIGURE 5.4-8 and FIGURE 5.4-9 are derived from the requirements in ANSI/VITA 65.0. For clarification, refer to ANSI/VITA 65.0 and its related documents.

T2-RUL-3800: HOST Backplanes **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 65.0 for conduction cooled modules
3. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

5.4.2.3.2 Interfaces

T2-RUL-3810: HOST Backplanes **shall** conform to the interface requirements defined in ANSI/VITA 65.0.

T2-RUL-2480: HOST Backplanes **shall** have a 1-inch slot pitch.

T2-OBS-0901: HOST Backplanes are designed for interfacing to HOST Modules with 1-inch pitch; however, HOST Modules with .8 inch and .85 inch pitches are also allowed.

T2-RUL-3820: HOST Backplane Payload, Switch, Power Supply, and Energy Storage Slots **shall** use alignment and keying pins called out in ANSI/VITA 46.0, Observation 7-22.

T2-RUL-3890: Power supply module slots **shall** use connectors defined in ANSI/VITA 62.0, Table F-1.

T2-REC-0047: Alignment pin keying information for HOST Backplanes **should** be documented.

T2-RUL-3910: Transmission components **shall** prohibit features that prevent installation of a HOST Module.

T2-RUL-3920: No additional non-COTS components **shall** be required to install a HOST Module.

5.4.2.3.3 6U Interface Requirements

T2-RUL-3830: HOST Backplane 6U Power Supply Module Slots **shall** be keyed in accordance to ANSI/VITA 62.0, Section 4.3.2 6U Slot Keying.

T2-RUL-3840: Key position 1 for HOST Backplane 6U Payload slots **shall** be set to 315 degrees.

T2-RUL-3850: Key position 1 for HOST Backplane 6U Switch slots **shall** be set to 315 degrees.

T2-OBS-0078: The numbering for the key positions is called out in ANSI/VITA 46.0, Rule 4-12.

T2-RUL-3880: 6U Payload and Switch slots **shall** use connectors defined in ANSI/VITA 46.0, Table 6-1, or the rugged equivalent RT2-R, unless the slot is utilized for a Module following SECTION 5.1.1.1.2.3.

T2-PER-3881: 6U Payload slots **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.2.3.

5.4.2.3.4 3U Interface Requirements

T2-RUL-3881: HOST Backplane 3U Power Supply Module Slots **shall** be keyed in accordance to ANSI/VITA 62.0, Section 4.3.1 3U Slot Keying.

T2-OBS-0911: The numbering for the key positions is called out in ANSI/VITA 46.0, Rule 4-12.

T2-RUL-3885: 3U Payload and Switch slots **shall** use connectors defined in ANSI/VITA 46.0, Table 5-1, or the rugged equivalent RT2-R, unless the slot is utilized for a Module following SECTION 5.1.1.1.3.7.

T2-PER-3882: 3U Payload slots **may** use connectors defined in ANSI/VITA 66.0 and ANSI/VITA 67.0 per SECTION 5.1.1.1.3.7.

5.4.2.3.5 Environmental Requirements

T2-RUL-3940: Conformal coating for HOST Backplanes **shall** be applied per IPC J-STD-001F.

T2-RUL-3950: Materials used for conformal coating **shall** conform to IPC-CC-830B and be included in QPDSIS-46058.

6 Glossary

Term	Definition
Analysis	Analysis is an element of verification that uses generally accepted technical methods including mathematical models or simulations, algorithms, charts, graphs, circuit diagrams, data, or other scientific principles and procedures to determine conformance with specified requirements. "Generally accepted", in this context, means in accordance with common design engineering practices.
Backplane Profile	A physical definition of a backplane implementation that includes details such as the number and type of slots that are implemented and the topologies used to interconnect them. Ultimately a Backplane Profile is a description of channels and buses that interconnect slots and other physical entities in a backplane.
Chassis Domain Inventory Information Record	Chassis Domain Inventory Information Records contain the hardware-specific information necessary to uniquely identify and verify the configuration of the HOST Chassis it represents. The information typically contained in Inventory Information Records includes serial number, part number, model, inventory number ("asset tag"), and the version numbers for any manufacturer-installed software or firmware.
Chassis Management Transmission Interface	The CMTI provides connectivity between Chassis Management entities (Chassis Managers, and IPMCs). The CMTI provides chassis management and utility capabilities such as health monitoring, status reporting, maintenance, system reset, system power-up/power-down management, and system recovery. The CMTI can share a physical transmission medium with other transmission interfaces but it remains logically distinct based upon the type of data that it carries.
Chassis Manager	The Chassis Manager is a software or firmware entity that manages IPMCs within the Chassis Domain. The Manager communicates with IPMC via the CMTI. This standard allows the usage of two kinds of Chassis Manager: an active Chassis Manager and a backup Chassis Manager.
Commercial-Off-the-Shelf	A commercial item sold in substantial quantities in the commercial marketplace and offered to the government under a contract or subcontract, without modification, in the same form in which it was sold in the marketplace.
Conformance Verification and Applicability Matrix	CVAM is an appendix in HOVM that contains entries for all HOST Tier 2 requirements. It identifies the requirement ID, applicability of the requirement to the specific types of components identified in the Tier 2 Standard, recommended verification method for the requirement, and other additional information as necessary, for each Tier 2 rule.

Term	Definition
Demonstration	Demonstration is an element of verification that involves the qualitative exhibition of functional performance. While test equipment might be required as part of the Demonstration setup, measurements are typically not required. Demonstration might also be used when requirements or specifications are given in statistical terms (e.g., average power consumption, mean time to repair, etc.).
External I/O Transmission Interface	The EIOTI provides a method for connecting Platform I/O and power signals to the SIOTI and SPDI where they can then be accessed by I/O processing and PSRs. The EIOTI will typically take the form of front and/or rear panel chassis I/O connection systems that utilize any combination of cabling, rigid printed wiring board (PWB), or flex PWB.
Functional Resources	FRs perform the main functions of the system. Functions may include but are not limited to processing of the I/O, image processing, data processing, general purpose processing, data storage, etc. These resources differ from PSRs and Chassis Management in that those architectural elements exist to support the FRs.
Field Replaceable Unit	An electronic hardware component that can be removed and replaced without sending the product to a repair facility. Throughout this Tier 2 HOST Standard, “FRU” should be interpreted as “HOST Module.”
HOST Backplane	A physical circuit card assembly that accepts HOST Plug-In Modules and provides access to the Transmission Interfaces.
HOST Chassis	A HOST Chassis is the aggregate collection of HOST Modules governed by a single Chassis Manager.
HOST Component	A physical device that is defined, in whole or part, by requirements in the HOST Standards. The HOST Components include but are not limited to HOST Enclosures, HOST Modules, HOST Transmission Components, and HOST External Interfaces.
HOST Enclosure	A physical chassis that holds together all of the HOST Components in a Target System implementation.
HOST External Interface	Physical connection between the HOST Transmission Components and the external system.
HOST Mezzanine Module	A HOST Component that contains functionality as defined by the HOST Resources and a physical form factor that conforms to the requirements of this HOST Tier 2 OpenVPX Standard for mezzanines.

Term	Definition
HOST Module	A HOST Component that contains logical and physical functionality as defined by the HOST Resources, utilizes one or more HOST Transmission Interfaces, and is visible to the Chassis Management Architecture. HOST Modules are managed by IPMC functionality. IPMCs exist at the Module Domain level to oversee a single HOST Module's configuration, BIT, fault logging, startup, etc. Examples of Tier 2 HOST Module implementations can include: printed wiring Plug-In Modules, mezzanine modules, power supply modules, etc.
HOST OpenVPX Verification Method	HOVM is a companion document that details the verification method information required for Tier 3 Specifications that conform to the requirements of the Tier 2 Standards document.
HOST Plug-In Module	A HOST Component that contains functionality as defined by the HOST Resources and plugs directly into a backplane.
Inspection	Inspection is an element of verification that involves an examination of the item/system or drawing form. Drawing forms are any controlled document that defines the product configuration for design, assembly, or Test. Inspection may include gauging or measurement.
Intelligent Platform Management Bus	Name for the architecture, protocol, and implementation of a special bus that interconnects the baseboard and chassis electronics and provides a communications media for system platform management information. It is defined by the Intelligent Platform Management Interface Specification (IPMI).
Module Profile	A physical mapping of ports onto a given Module's backplane Connectors and protocol mapping(s), as appropriate, to the assigned Port(s). This definition provides a first-order check of operating compatibility between Modules and slots as well as between multiple Modules in a Chassis. Module Profiles achieve the physical mapping of ports to backplane connectors by specifying a Slot Profile. Multiple Module Profiles can specify the same Slot Profile.
Platform	A vehicle or weapons system on which a HOST based system will be installed (e.g. an aircraft).
Power Supply Resource	PSRs transform Target System power into chassis power that is supplied to HOST Modules via the system power distribution Interface. Modules that implement PSRs must support the Power Distribution Interface since that is the exclusive power distribution interface for HOST Modules.
Requirements Verification Matrix	The RVM lists verification methods for both the HOST and performance (all platform derived requirements) requirements for the Tier 3 component being defined.

Term	Definition
Slot Profile	A physical mapping of ports onto a given slot's backplane connectors. These definitions are often made in terms of Pipes. Slot Profiles also give the mapping of Ports onto Plug-In Module's backplane connectors. Unlike Module Profiles, a Slot Profile never specifies protocols for any of the defined Ports.
System Communications Transmission Interface	The SCTI carries general communications data between resources. General communications data consists of resource coordination and data messages required for general computing performance. The SCTI does not carry Platform I/O signals between resources. The SCTI can share a physical transmission medium with other Transmission Interfaces but it remains logically distinct based upon the type of data that it carries. The SCTI could be implemented as an address mapped parallel bus, a packet-switched network, or any number of other communications methods.
System I/O Transmission Interface	The SIOTI connects I/O signals between the EIOTI and I/O resources. The SIOTI does not carry general communications data between resources (i.e. data allocated to the SCTI).
System Power Distribution Interface	The SPDI distributes power from the Power Supply modules within the PSR to all modules requiring power. The power specifications and transmission methods are specific to a Tier 2 core technology standard.
Test	Test is an element of verification designed to provide data on functional features, performance, or equipment operation under fully controlled and traceable conditions. Test generally use special instrumentation or test equipment to obtain accurate the quantitative data for Analysis. The data is used to evaluate quantitative characteristics. Testing implicitly requires Analysis of the resulting test data.
Target System	A HOST based aggregation of components/modules intended to carry out a defined function on a Platform (e.g. a mission computer).

7 Acronyms

ATCA – Advanced Telecommunications Computing Architecture

ChMC – Chassis Manager Controller

CMTI – Chassis Management Transmission Interface

COTS – Commercial-Off-the-Shelf

CVAM – Conformance Verification and Applicability Matrix

EIOTI – External I/O Transmission Interface

FP – Fat Pipe

FR – Functional Resource

FRU – Field Replaceable Unit

HOST – Hardware Open System Technologies

HOVM – HOST OpenVPX Verification Methods

IPMB – Intelligent Platform Management Bus

IPMC – Intelligent Platform Management Controller

IPMI – Intelligent Platform Management Interface

JTAG – Joint Test Action Group

MRI – Manager Redundancy Interface

OEM – Original Equipment Manufacturer

OFP – Operational Flight Program

PCI – Peripheral Component Interconnect

PCIe – Peripheral Component Interconnect Express

PMC – PCI Mezzanine Card

PSM – Power Supply Module

PSR – Power Supply Resource

PWB – Printed Wiring Board

RVM – Requirements Verification Matrix

SATA – Serial Advanced Technology Attachment

SCTI – System Communications Transmission Interface

SDR – Sensor Data Record

SEL – System Event Log

SIOTI – System I/O Transmission Interface

SPDI – System Power Distribution Interface

UD – User Defined

UTC – Coordinated Universal Time

UTP – Ultra Thin Pipe

VA – Verification Authority

XMC – Switched Mezzanine Card