HARDWARE OPEN SYSTEMS TECHNOLOGIES

Hardware Open Systems Technologies OpenVPX Core Technology Tier 2 Standard

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1 Overview

1.1 Objective

The *Hardware Open System Technologies* (HOST) OpenVPX Core Technology Tier 2 Standard applies OpenVPX embedded computing technologies to the HOST Tier 1 Standard architecture. This document introduces the application of OpenVPX as a Core Technology Standard, defines the conventions and conformance standards used in the document, and defines specific requirements of this Core Technology Standard.

1.2 HOST– OpenVPX Core Technology

The HOST OpenVPX Core Technology Standard defines technical requirements applying OpenVPX embedded computing technologies to the HOST Architecture. HOST Tier 2 standards are *Platform* agnostic, so this standard does not incorporate specific requirements of *Target Systems*. The goals of this HOST Core Technology Standard are to:

- Apply OpenVPX embedded computing technologies and leverage ANSI/VITA 46.11 for hardware system management to define Target System agnostic requirements
- Facilitate OpenVPX computing hardware interoperability and reuse
- Facilitate the extensive use of OpenVPX *Commercial-Off-the-Shelf* (COTS) components
- Enable the derivation of HOST Tier 3 Specifications from the combination of the HOST Tier 1 Standard, HOST Tier 2 Standard, and Target System requirements

Throughout the document, the standard is referred to interchangeably by the following terms: “HOST Tier 2 Standard,” “Tier 2 HOST Standard,” and “Tier 2 Core Technology Standard.”

1.3 Referenced Documents

ANSI/VITA 42.0-2008 (R2014), Switched Mezzanine Card (XMC)

ANSI/VITA 42.3-2006 (R2014), XMC PCI Express Protocol Layer Standard

ANSI/VITA 46.0-2019, VPX Base Standard

ANSI/VITA 46.6-2013, Gigabit Ethernet Control Plane on VPX

ANSI/VITA 46.9-2017, PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard

ANSI/VITA 46.11-2015, System Management on VPX

ANSI/VITA 47-2005, Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard

ANSI/VITA 48.2-2010, Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to ANSI/VITA VPX

ANSI/VITA 62.0-2012, Modular Power Supply Standard

ANSI/VITA 65.0-2019 Draft, OpenVPX (VITA65d0-draft-4d07-gr2019-03-26)

ANSI/VITA 65.1-2019 Draft, OpenVPX System Standard – Profile Tables (VITA65d1-2d07-gr2019-03-26)

ANSI/VITA 66.0-2016, Optical Interconnect on VPX – Base Standard

ANSI/VITA 67.0-2012, Coaxial Interconnect on VPX – Base Standard

ANSI/VITA 67.3-2016, Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane

IEEE 802.3-2012 (December 28, 2012), IEEE Standard for Ethernet

IEEE 1101.2-1992 (January 31, 2008), IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards

IEEE 1386.1-2001 (June 14, 2001), IEEE Standard Physical and Environmental Layers for PCI Mezzanine

Intelligent Platform Management Interface (IPMI) Specification Version 2.0, Revision 1.1, dated 01 October 2013

IPC J-STD-001F (July 2014), Requirements for Soldered Electrical and Electronic Assemblies

IPC-CC-830B with Amendment 1 (October 2008), Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPMI Platform Management FRU Information Storage Definition Version 1.0, Revision 1.2, dated 28 February 2013

QPDSIS-46058 Insulating Compound, Electrical, dated 22 June 2017

2 Implementation

This Tier 2 HOST Standard governs the implementation of HOST conformant *system*s utilizing the ANSI/VITA 65.0 OpenVPX System Specification and related embedded computing standards. More specifically, this Tier 2 Architecture defines the implementation of the following HOST Architecture elements with OpenVPX as the core technology for hardware. ANSI/VITA 46.11 and IPMI standards are leveraged for hardware management.

2.1 Hardware System Management

Hardware System Management Architecture establishes an autonomous subsystem that provides application independent hardware management and monitoring capabilities for the module, chassis, and system domains. Hardware System Management implements Sensor Management, System/Module Inventory and Configuration, SW/FW Management, Field Replaceable Unit (FRU) Recovery, and Diagnostic Management capabilities. This Tier 2 HOST Standard extends ANSI/VITA 46.11 and IPMI standards to define the required data exchanges and Hardware System Management messages.

2.2 Hardware Implementation

This Tier 2 HOST Standard standardizes hardware components and their interfaces to facilitate interoperability between the components residing in an Enclosure.

2.2.1 HOST Components

HOST Components are divided into four main categories: Modules, External Interfaces, Transmission Interfaces, and the Enclosure.

2.2.1.1 HOST Modules

HOST Modules are implemented as *Plug-In Modules* or as *HOST Mezzanine Modules*.

HOST Plug-In Modules are implemented using ANSI/VITA 65.0/ANSI/VITA 48.2 Conduction-cooled VPX Modules, and ANSI/VITA 62.0 Power Supplies. VPX Modules include Payloads, External I/O Modules, Switches, and other miscellaneous Module types listed in ANSI/VITA 65.0.

HOST Mezzanine Modules are implemented using ANSI/VITA 42.0/42.3 *Switched Mezzanine Cards* (XMC) Standard and IEEE 1385 PCI Mezzanine Cards (PMC).

2.2.1.2 HOST External Interface

HOST External Interfaces provide the physical connection, which transfer signals and power between the HOST Transmission Components and the external system.

2.2.1.3 Transmission Interface

Transmission Interfaces are responsible for the logical and physical connectivity within the system. For this Tier 2 core technology, Transmission Interfaces are implemented utilizing backplanes composed of HOST-specific and ANSI/VITA 65.0 design elements.

2.2.1.4 HOST Enclosure

The *HOST Enclosure* is implemented utilizing ANSI/VITA 48.2 and ARINC 404 1-ATR Enclosure design elements.

2.3 Resource Implementation

Although this Tier 2 HOST Standard is based primarily upon the use of OpenVPX as the core technology, it will further define requirements for making OpenVPX components HOST conformant. Therefore, a component that is OpenVPX conformant is not necessarily HOST conformant.

FIGURE 2.3-1 shows an example of how the resources could be implemented on different HOST Modules.

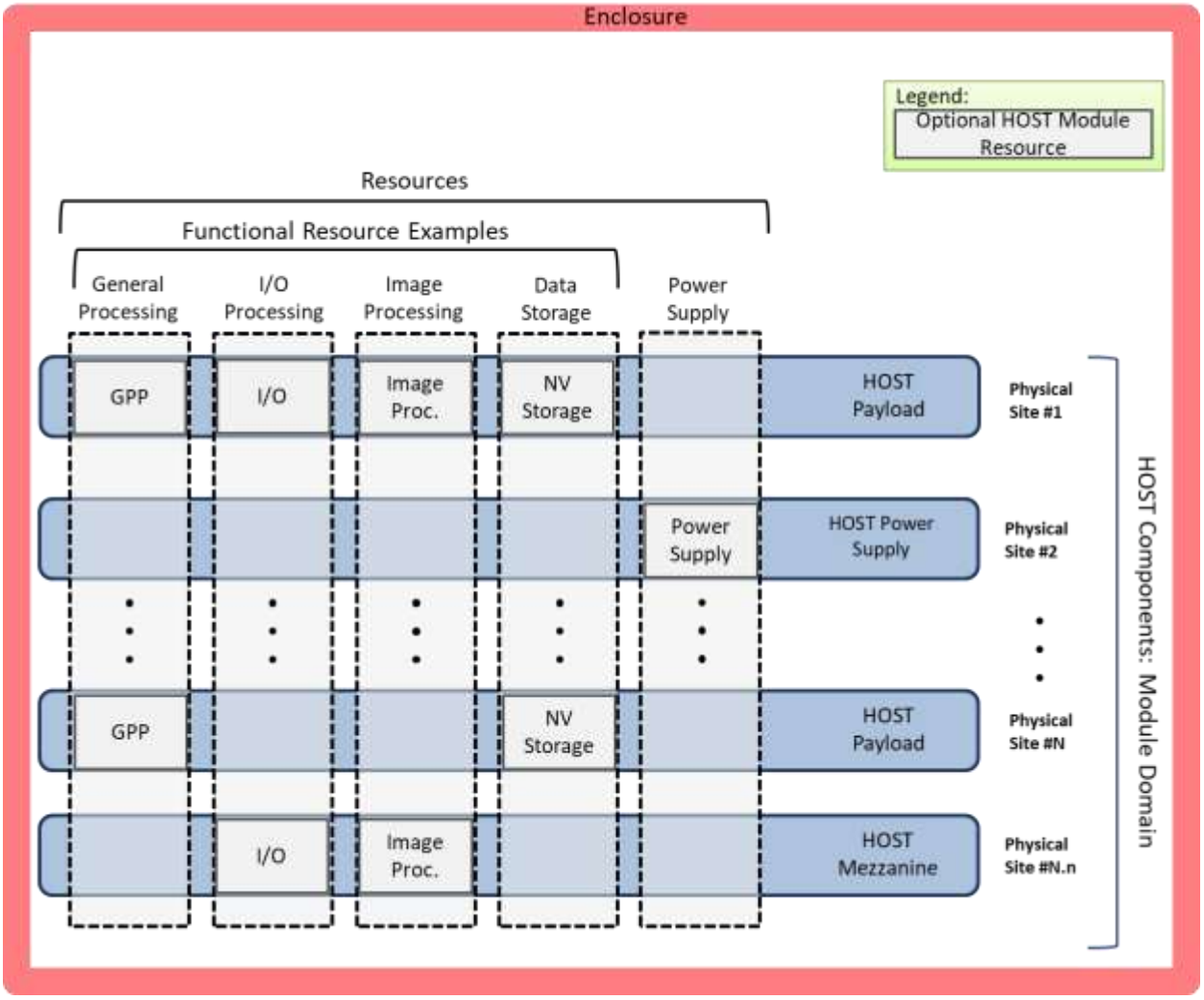


Figure 2.3-1 – Resource Implementation Example

In FIGURE 2.3-1 the HOST Payload Module is based on an ANSI/VITA 65.0 Plug-In Module, the HOST Mezzanine could be either a PMC or XMC module, and the HOST Power Supply is based on an ANSI/VITA 62.0 Power Supply Plug-In Module. (Note: Terminology in this standard follows the ANSI/VITA standard where a mezzanine is interchangeably called a card or module.)

3 Guidelines

3.1 Typography

The following typographical conventions are used throughout this document:

- *Italics* – Indicates a term defined in the glossary or for emphasis (occurs on first instance).
- **Bold** – Indicates identifiers and their terms (ex: “shall”, “should”, “may”) as defined in SECTION 3.2.
- SMALL CAPS - Cross-reference to another section, figure, or table in this document.

3.2 Identifier

To avoid confusion, many of the paragraphs in this standard are provided with an identifier that indicates the type of information that the paragraph contains and is uniquely identifiable.

These identifiers are of the format **Tk-nnn-xxxx** where:

- k is equal to the HOST Tier that the identifier is from
- nnn is an indicator of the type of content, where:
  - RUL is a rule
  - REC is a recommendation
  - PER is a permission
  - OBS is an observation
- xxxx is a sequence number

The types of content are reserved for specific use as defined in subsequent sections.

References to a section or paragraph from an external source that are included in a statement with an identifier will also contain all lower level sections and paragraphs.

Any text not provided with an identifier is to be interpreted as descriptive in nature. This text will be written in either a descriptive or a narrative style.

3.2.1 Rule

Compliance with rules is mandatory. Rules always include the term “shall.” Rules are expressed in some combination of text, figures, tables, or drawings. All rules will be followed to ensure compatibility across interfaces.

3.2.2 Recommendation

Compliance with Recommendations is optional. Recommendations always include the term “should.” Recommendations are used to convey implementation advice based on the community’s collective knowledge base. Recommendations found in this standard are provided to designers to reduce their learning curve.

3.2.3 Permission

Compliance with Permissions is optional. Permissions always include the term “may.” In some cases, a rule does not specifically prohibit a certain design approach, but the reader might be left wondering whether that approach might violate the spirit of the rule or whether it might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable.

3.2.4 Observation

Observations do not offer any specific advice. They are provided to enhance comprehension and usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands the spirit of the rule.

4 HOST Conformance

Defining conformance and creating a method for verifying and certifying HOST products is vital to establishing an effective standard. Certification provides formal recognition of conformance to a HOST standard or specification. Without the associated conformance criteria and processes, there is no assurance that a supplier has developed or implemented products or solutions according to the approved HOST Technical Standards and Specifications. Verification provides evidence of conformance to a HOST Technical Standard or Specification, which allows:

- Buyers to specify and successfully procure hardware from vendors who provide solutions that conform to the HOST Specifications and Standards.
- System Integrators to make and substantiate clear claims of conformance to HOST Specifications and/or Standards.
- Hardware component suppliers to make and substantiate clear claims of conformance to HOST Specifications.

The government will establish conformance criteria and define an associated Conformance Program for the HOST Tier 3 Specifications and HOST Components.

The conformance assessment is intended to certify compliance with HOST requirements and is not intended to ensure a component or system will function as intended in its final application. Conformance assessment is not meant to assist with or replace developmental or operational test.

4.1 HOST Conformance Program

The HOST Conformance Program will have two primary functions:

1) Verification that a newly developed or revised Tier 3 Specification complies with the requirements of the applicable HOST Tier 2 Standard.
2) Verification that a hardware component complies with the requirements of the applicable HOST Tier 3 Specification.

4.1.1 HOST Conformance Program Terminology

HOST Conformant is used for an article an article if and only if the Tier 3 Specification and/or Module has completed the HOST Conformance Verification Process and been Gatekeeper Approved. For a module, this entails demonstration of strict adherence to a HOST Conformant Tier 3 Specification's requirements. For a Tier 3 Specification, this requires proper documentation of the requirements levied on a module in accordance with the tenets of the Tier 3 Specification Guide.

HOST Verification is the act of determining the conformance of a HOST product to the applicable HOST technical standard or specification requirements. The applicable Tier 2 Standards and Tier 3 Specification will have associated matrices that recommend or specify a verification method for each rule. Verification will be carried out by the agency responsible for developing the HOST product being verified. Results and artifacts of the verification will be submitted to a *Verification Authority* (VA). The VA will review the verification results and artifacts to make a determination on whether the verification process was sufficiently correct and complete to show conformance to the next higher level specification or standard.

HOST Registration is the process of listing Certified HOST Tier 3 Specifications and Components in a public listing known as the HOST Registry.

4.1.2 Verification Methods

HOST Component requirements will be based on one of the following conformance methods: *Inspection*, *Analysis*, *Demonstration*, or *Test*.

4.1.3 HOST OpenVPX Verification Methods Document

The *HOST OpenVPX Verification Methods* (HOVM) document provides two different types of information in support of this Tier 2 standard. First, the HOVM identifies which Tier 2 rules pertain to HOST Modules and which rules pertain to other portions of the HOST system such as the Backplane or Enclosure. Second, the HOVM provides detailed verification method information required for Tier 3 module specifications that conform to the requirements of this document.

The HOVM contains a *Conformance Verification and Applicability Matrix (CVAM)*. The CVAM will include entries for all HOST Tier 2 requirements and identify, at a minimum, the following details for each Tier 2 rule: requirement ID, an indication of whether the rule pertains to a HOST Module or the HOST system, applicability to the specific types of components identified in the Tier 2 Standard, recommended verification method for the requirement, and additional information as necessary. The HOVM also defines the types of documentation that are required for verification of a Tier 3 Specification.

4.1.4 HOST Tier 3 Specification Conformance

Tier 3 Specifications will be verified to show conformance to this Tier 2 Standard. The agency authoring the Tier 3 Specification will perform and document a requirements trace to show that all applicable rules of this document have been flowed down to the Tier 3 Specification. In addition, a check will be made to verify that the Tier 3 Specification's *Requirements Verification Matrix* (RVM) covers all of the requirements identified in the Tier 3 Specification. The Tier 3 RVM will be checked to verify that it lists the appropriate verification methodology for each requirement per the CVAM contained in the HOVM. The submitting agency will provide the results of their verification efforts and supporting documentation to be reviewed by the VA. Upon successful completion of the HOST Tier 3 conformance process, the Tier 3 Specification will be published.

4.1.5 HOST Component Conformance

Components will be verified to show conformance to the applicable HOST Tier 3 Specification. Verification methods for component requirements will be identified in an RVM included in the Tier 3 Specification. The submitting agency will perform verification of the developed product to show conformance to the Tier 3 Specification. The submitting agency will provide the results of their verification efforts and supporting documentation to be reviewed by the VA. Upon successful completion of the HOST conformance process and review by the VA, the component data will be entered into the HOST Registry.

T2-RUL-0005: HOST Modules **shall** conform to one or more HOST Tier 3 Specifications.

T2-RUL-0008: Documentation for all Tests conducted, including environmental, to show conformance to HOST rules/requirements **shall** include, at a minimum, Test procedures, Test equipment information, collected Test data, and Test results.

T2-OBS-0044: Requiring documentation for tests conducted for conformance is in line with industry practices for compliance, for example ANSI/VITA 65, Rule 2.2.4-1.

T2-PER-0001: Non-Module HOST Components **may** conform to one or more HOST Tier 3 Specifications.

T2-RUL-0016: Level A Conformant Modules **shall** implement all applicable rules within this standard.

T2-RUL-0017: Level B Conformant Modules **shall** implement all rules except SECTION 5.3 Hardware System Management Rules.

T2-OBS-0041: The difference between a Level A and Level B Conformant Modules essentially comes down to whether the Module supports ANSI/VITA 46.11 based Hardware System Management, per SECTION 5.3 of this Standard. Level A Conformant Modules support all of the HOST System Management requirements, while Level B Conformant Modules do not. Note that HOST Mezzanine Modules are Level A by default due to not having any applicable rules in SECTION 5.3.

4.1.6 Requirements Verification Matrix

The Tier 3 Specification will include an RVM. The purpose of the RVM is to identify the required verification method for each Tier 3 Specification requirement. The RVM will identify whether or not each Tier 3 requirement traces to a HOST Tier 2 Standard requirement. In addition, the RVM will include the required verification method, an indication on whether each Tier 3 requirement was derived from this HOST Tier 2 Standard, the product specification, or both. For clarity, the RVM shall include entries for Tier 2 rules that are not applicable to the HOST component. These rules will be identified as not applicable.

T2-RUL-0001: A HOST Tier 3 Specification conforming to this standard **shall** include an RVM that includes one or more entries for each rule of this standard.

T2-RUL-0002: For each Tier 3 requirement, the Tier 3 RVM **shall** indicate whether the requirement was derived from a HOST Tier 2 rule, the product specification or both.

T2-RUL-0018: For each Tier 3 requirement that traces to one or more HOST Tier 2 rules, the Tier 3 RVM **shall** identify which Tier 2 rules trace to that Tier 3 requirement.

T2-RUL-0019: For each Tier 3 requirement, the Tier 3 RVM **shall** specify the required verification method.

T2-RUL-0004: For each Tier 2 rule applicable to the type of component specified in Tier 3, the Tier 3 Specification **shall** identify the required artifacts and any additional information required for verification.

T2-RUL-0021: For each Tier 2 rule that does not apply to the HOST component type specified by the Tier 3 as specified by the CVAM, the RVM **shall** contain an entry which identifies that Tier 2 rule as not applicable.

5 Tier 2 Standard Requirements

5.1 HOST Module Requirements

This HOST Tier 2 Core Technology Standard implements HOST Modules as 6U and 3U OpenVPX Plug-In Modules, ANSI/VITA 62.0 Power Supply Plug-In Modules, and PMC/XMC Mezzanine Modules. HOST Plug-In Modules consist of HOST VPX Modules and HOST *Power Supply Modules* (PSM) that connect (plug-in) directly to the *HOST Backplane* component. HOST Payload Modules are used to implement the *Functional Resources* (FR) and/or act as carriers of HOST Mezzanine Modules. HOST Switch Modules provide *System Communications Transmission Interface* (SCTI) interconnection between HOST Payload Modules. HOST External I/O Modules are used to interface with platform I/O and convert the I/O into standard protocols communicating with other VPX Modules throughout a system. HOST Power Supply Modules transform Platform power into system power for use by HOST VPX modules.

The hierarchy of rules for the various HOST Module types is shown in FIGURE 5.1-1.

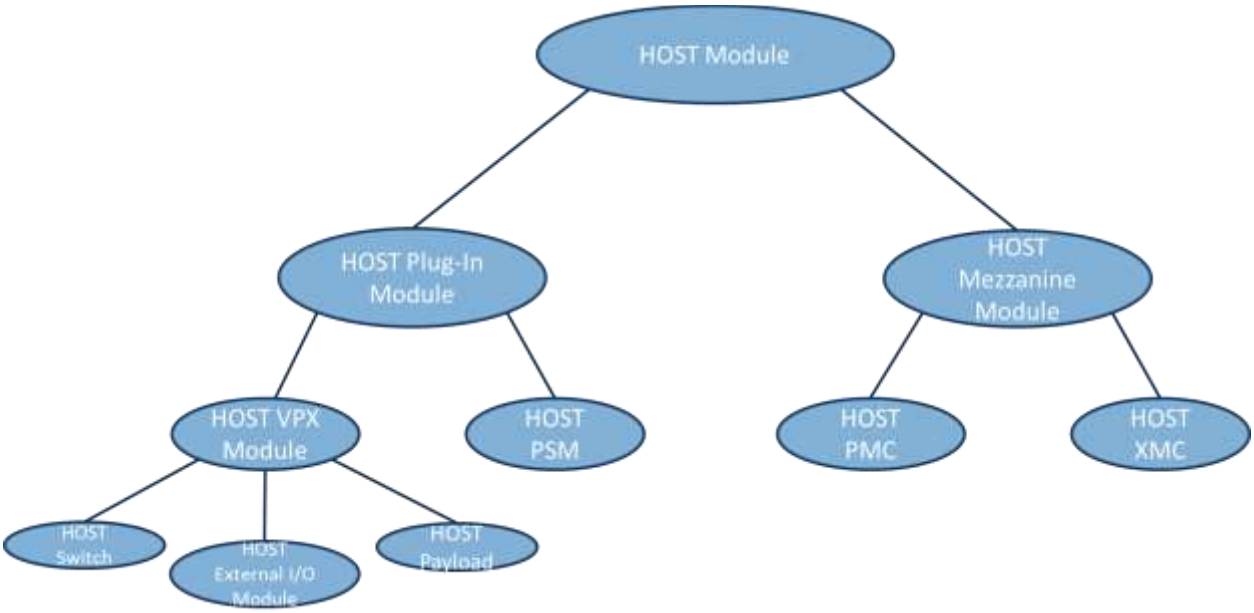


Figure 5.1-1 – HOST Module Rules Hierarchy

The module hierarchy clarifies which rules each module type must follow. For example, a HOST Switch must follow any rules levied on HOST Switches, HOST VPX Modules, HOST Plug-In Modules, and HOST Modules, but a HOST Switch does not have to follow rules levied on HOST Payloads, HOST PSMs, or HOST Mezzanines Modules.

T2-RUL-0010: For this Tier 2 Core Technology Standard a HOST Module **shall** be defined as a VPX Module, Power Supply Module, PMC Mezzanine Module, or an XMC Mezzanine Module.

T2-RUL-0011: VPX Modules and Power Supply Modules **shall** conform to the requirements of HOST Plug-In Modules.

T2-RUL-0012: PMC and XMC Modules **shall** conform to the requirements of HOST Mezzanine Modules.

T2-RUL-0020: A HOST Module **shall** conform to interface requirements of the *Chassis Management Transmission Interface* (CMTI) per SECTION 5.4.1.5.

T2-PER-0010: A HOST Module **may** utilize the *System I/O Transmission Interface* (SIOTI) per SECTION 5.4.1.3.

T2-RUL-0030: A HOST Module **shall** conform to the interface requirements of the *System Power Distribution Interface* (SPDI) per SECTION 5.4.1.6.

T2-RUL-0052: HOST Modules **shall** leave signals HOST defines as reserved unconnected.

T2-PER-0012: A HOST Module **may** have only a subset of the SPDI voltages defined within the OpenVPX Utility Plane as an input.

T2-RUL-0031: If a HOST Module uses only a subset of the SPDI voltages defined within the OpenVPX Utility Plane as an input, the HOST Module **shall** leave the pins meant for the unused voltages as Reserved.

5.1.1 HOST Plug-In Module Requirements

T2-RUL-0121: HOST Plug-In Module requirements **shall** be applied using the following order of precedence:

1. Requirements of SECTION 5.1.1.1 VPX Modules and SECTION 5.1.1.2 Power Supply Modules
2. Requirements of SECTION 5.1.1 HOST Plug-In Module Requirements

T2-RUL-0053: HOST Plug-In Modules **shall** follow ANSI/VITA 46.0, Rule 3-1 regarding safety ground.

T2-RUL-0057: HOST Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.9 3.3V_AUX.

T2-RUL-0058: HOST Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.11 SYSRESET*.

T2-RUL-0059: HOST Plug-In Modules **shall** draw no more than 1 mA from VBAT per Rule 4-56.1 of ANSI/VITA 46.0.

T2-RUL-0061: If implementing the 12V_AUX +/-, HOST Plug-In Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.10 12V_AUX.

5.1.1.1 VPX Modules

5.1.1.1.1 Common 6U and 3U VPX Module Requirements

T2-RUL-0122: VPX Module requirements **shall** be applied using the following order of precedence:

1. Requirements for a specific Module Form Factor and Profile Number, e.g. SECTION 5.1.1.1.2.3.1 3U Payload Profile 1: PAY-2F2U
2. Requirements for a specific Form Factor and Profile Type, e.g. SECTION 5.1.1.1.2.3 3U Payload Module Requirements
3. Requirements common to a Profile Type, e.g. SECTION 5.1.1.1.3.1 Common 6U and 3U HOST Switch Requirements
4. Requirements for a VPX Module in SECTION 5.1.1.1.1 Common 6U and 3U VPX Module Requirements

T2-RUL-0531: VPX Modules **shall** implement the requirements of ANSI/VITA 65.0, Section 3.7 (OpenVPX ANSI/VITA 46.0 Connector P0/J0 and P1/J1 Connector Pin Assignments).

T2-RUL-0055: VPX Modules **shall** be designed to accommodate any combination of power supply power up and power down sequences without causing board failure.

T2-RUL-0535: VPX Modules **shall** follow the rules of ANSI/VITA 46.0, Section 4.8.3 System Controller and ANSI/VITA 65.0, Section 3.4.1.

T2-RUL-0140: VPX Modules **shall** conform to the applicable interface requirements of the SCTI per SECTION 5.4.1.2.

T2-OBS-0100: The OpenVPX Data Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-OBS-0101: The OpenVPX Expansion Plane is part of the SCTI as defined in SECTION 5.4.1.2.

T2-RUL-0240: VPX Modules **shall** implement the requirements of ANSI/VITA 65.0, Section 6.3.3, (User Defined).

T2-OBS-0150: The OpenVPX User Defined connections are part of the SIOTI as defined in SECTION 5.4.1.3.

T2-OBS-0120: Reserved signals cannot be utilized for any other purpose (such as user I/O).

T2-REC-0010: When single-ended user defined signals that require tight tolerances, precise values, and/or very short rise times, are routed over pins intended for differential pairs, just the positive pin of a pair **should** be used for the signal, with the negative pin of the pair grounded. This is to prevent potential crosstalk of the single-ended user defined signals.

T2-OBS-0080: The SPDI supports the battery backup power rail per ANSI/VITA 65.0, Section 3.2.2 and ANSI/VITA 46.0, Section 4.9.2.

T2-OBS-0081: Refer to recommendations of ANSI/VITA 65.0, Section 3.2.4 on inrush (surge) current.

T2-PER-0061: VPX Modules **may** implement 10GBASE-KR on the UTPs.

T2-RUL-0511: VPX Modules using 10GBASE-KR **shall** comply with ANSI/VITA 65.0, Section 5.1.7.

T2-PER-0072: VPX Modules **may** implement 25GBASE-KR on the UTPs.

T2-RUL-0512: VPX Modules using 25GBASE-KR **shall** comply with ANSI/VITA 65.0, Section 5.1.15.

T2-OBS-0019: The OpenVPX Control Plane is part of both the SCTI and CMTI as defined in SECTION 5.4.1.2 and SECTION 5.4.1.5.

T2-PER-0039: VPX Modules **may** utilize a newer generation of *Peripheral Component Interconnect Express* (PCIe) than what is called out in the Module Profile.

5.1.1.1.2 Payload Modules

This Tier 2 HOST Standard utilizes a set of HOST-defined OpenVPX *Slot Profiles* and *Module Profiles* for all HOST Payload Modules. The Slot Profile maps OpenVPX ports to the HOST Backplane's connector interface. The Module Profile specifies which protocols are mapped to the ports defined in the Slot Profile.

5.1.1.1.2.1 Common Payload Module with Mezzanine Site Requirements

T2-RUL-0080: Payload Modules with PMC mezzanine sites **shall** conform to the carrier board, referred to as a host board in IEEE 1386.1, requirements of IEEE 1386.1.

T2-RUL-0090: Payload Modules with XMC mezzanine sites **shall** conform to the carrier board requirements of ANSI/VITA 42.0, XMC.

T2-OBS-0010: Compatibility with the PMC/XMC communications protocols is defined by the SCTI in SECTION 5.4.1.2.

T2-OBS-0020: Compatibility with the PMC/XMC power interfaces is defined by the SPDI in SECTION 5.4.1.6.

T2-OBS-0030: It is possible for a single mezzanine site to be compatible with both XMC and PMC mezzanine formats.

T2-OBS-0040: Mezzanine connector pinout requirements for Payload Modules with PMC Mezzanine sites are specified by IEEE Std. 1386.1 Section 5.2.

T2-OBS-0050: Voltage keying requirements for Payload Modules with PMC Mezzanine sites are specified by IEEE Std. 1386.1 Section 4.2.

T2-OBS-0060: Mezzanine connector pinout requirements for Payload Modules with XMC Mezzanine sites are specified by ANSI/VITA 42.0 Section 5-1.

T2-OBS-0070: It is possible for Payload Modules to be mezzanine carriers that do not natively contain any resources. In those cases, the Payload Module may only contain the bridges required to attach the PMC/XMC modules to the SCTI and CMTI.

T2-RUL-0100: Payload Module mezzanine sites configured to support a XMC Mezzanine **shall** implement the secondary XMC connector ground pins in accordance with ANSI/VITA 42.0 Table 5-4, Secondary XMC Connector Pin Definition, even if the signals of the Secondary connector are not used.

5.1.1.1.2.2 6U Payload Module Requirements

T2-RUL-0070: 6U Payload Modules **shall** conform to the 6U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0051: 6U Payload Modules **shall** follow ANSI/VITA 65.0, Section 12.1.2 with regards to Power Voltages and System Management.

T2-OBS-0079: Refer to ANSI/VITA 65.0, Recommendation 12.1.1.2-1 regarding maximum module power draw.

T2-RUL-0251: 6U Payload Modules **shall** conform to one of the 6U Payload Profiles as listed in SECTION 5.1.1.1.2.2.

5.1.1.1.2.2.1 6U Payload Profile 1: PAY-4F1Q2U2T

T2-RUL-0249: 6U Payload Profile 1 Modules **shall** conform to the Slot Profile SLT6-PAY-4F1Q2U2T-10.2.1 per ANSI/VITA 65.0, Section 10.2.1.

T2-RUL-0200: If a 6U Payload Profile 1 Module implements the Control Plane thin pipes, a Payload Module **shall** use the Control Plane thin pipes exclusively as part of the SIOTI.

T2-REC-0001: 6U Payload Profile 1 Modules **should** use the Control Plane thin pipes for debug.

T2-RUL-0250: 6U Payload Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-PAY-4F1Q2U2T-12.2.1-8
- MOD6-PAY-4F1Q2U2T-12.2.1-14
- MOD6-PAY-4F1Q2U2T-12.2.1-15
- MOD6-PAY-4F1Q2U2T-12.2.1-19

5.1.1.1.2.2.2 6U Payload Profile 2: PAY-4F1Q1H4U1T1S1S1TU2U2T1H

T2-RUL-0032: 6U Payload Profile 2 Modules **shall** conform to the Slot Profiles SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-n per ANSI/VITA 65.0, Section 10.6.3.

T2-RUL-0101: 6U Payload Profile 2 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-0
- SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-1
- SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-2

T2-RUL-0033: If a 6U Payload Profile 2 Module implements the Control Plane thin pipes, a Payload Module **shall** use the Control Plane thin pipes exclusively as part of the SIOTI.

T2-REC-0004: 6U Payload Profile 2 Modules **should** use the Control Plane thin pipes for debug.

T2-RUL-0034: 6U Payload Profile 2 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-1
- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-2
- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-3
- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-4
- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-5
- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-6
- MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-7

5.1.1.1.2.2.3 6U Payload Profile 3: PAY-4F2Q1H4U1T1S1S1TU2U2T1H

T2-RUL-0035: 6U Payload Profile 3 Modules **shall** conform to the Slot Profiles SLT6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-10.6.4-n per ANSI/VITA 65.0, Section 10.6.4.

T2-RUL-0102: 6U Payload Profile 3 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-10.6.4-0
- SLT6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-10.6.4-1
- SLT6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-10.6.4-2

T2-RUL-0036: If a 6U Payload Profile 3 Module implements the Control Plane thin pipes, a Payload Module **shall** use the Control Plane thin pipes exclusively as part of the SIOTI.

T2-REC-0005: 6U Payload Profile 3 Modules **should** use the Control Plane thin pipes for debug.

T2-RUL-0037: 6U Payload Profile 3 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-1
- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-2
- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-3
- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-4
- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-5
- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-6
- MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-12.6.4-7

5.1.1.1.2.2.4 6U Payload Module with Mezzanine Site Requirements

T2-RUL-0110: 6U Payload Module mezzanine sites configured to exclusively support a PMC Mezzanine **shall** conform to ANSI/VITA 46.9, Section 5.1 (P64S) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0120: 6U Payload Module mezzanine sites configured to exclusively support a XMC Mezzanine **shall** conform to ANSI/VITA 46.9, Section 5.4 (X38S+X8D+X12D) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0130: 6U Payload Module mezzanine sites configured to support both PMC and XMC Mezzanines **shall** conform to ANSI/VITA 46.9, Section 5.2 (P64S+X12D) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

5.1.1.1.2.3 3U Payload Module Requirements

T2-RUL-0142: 3U Payload Modules **shall** conform to the 3U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0141: 3U Payload Modules **shall** follow ANSI/VITA 65.0, Section 16.1.2 with regards to Power Voltages and System Management.

T2-OBS-0154: Refer to ANSI/VITA 65.0, Recommendation 16.1.1.2-1 regarding maximum module power draw.

T2-RUL-0159: 3U Payload Modules **shall** conform to one of the 3U Payload Profiles as listed in SECTION 5.1.1.1.2.3.

5.1.1.1.2.3.1 3U Payload Profile 1: PAY-2F2U (Deprecated)

This profile is marked as deprecated and will be removed in a future version of this standard.

T2-RUL-0160: 3U Payload Profile 1 Modules **shall** conform to the Slot Profile SLT3-PAY-2F2U-14.2.3 per ANSI/VITA 65.0, Section 14.2.3.

T2-RUL-0161: 3U Payload Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-2F2U-16.2.3-3
- MOD3-PAY-2F2U-16.2.3-5
- MOD3-PAY-2F2U-16.2.3-10
- MOD3-PAY-2F2U-16.2.3-11

T2-PER-0050: 3U Payload Profile 1 Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

T2-RUL-0157: 3U Payload Profile 1 Modules containing backplane USB interfaces called out in ANSI/VITA 65.1 MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15 **shall** populate pins for the USB interface(s) in accordance with the USB usage defined in ANSI/VITA 65.0 Table 14.2.16-2.

T2-RUL-0158: 3U Payload Profile 1 Modules containing backplane SATA (Serial Advanced Technology Attachment) interfaces called out in ANSI/VITA 65.1 MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15 **shall** populate pins for the SATA interface in accordance with the SATA usage defined in ANSI/VITA 65.0 Table 14.2.16-2.

T2-RUL-0179: 3U Payload Profile 1 Modules containing backplane DisplayPort interfaces called out in ANSI/VITA 65.1 MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15 **shall** populate pins for the DisplayPort interface(s) in accordance with the DisplayPort usage defined in ANSI/VITA 65.0 Table 14.2.16-2.

5.1.1.1.2.3.2 3U Payload Profile 2: PAY-1F1F2U (Deprecated)

This profile is marked as deprecated and will be removed in a future version of this standard.

T2-RUL-0162: 3U Payload Profile 2 Modules **shall** conform to the Slot Profile SLT3-PAY-1F1F2U-14.2.4 per ANSI/VITA 65.0, Section 14.2.4.

T2-RUL-0163: 3U Payload Profile 2 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-1F1F2U-16.2.4-8

T2-PER-0055: 3U Payload Profile 2 Modules utilizing Ethernet on the Data Plane **may** use 40GBase-KR4 Ethernet per ANSI/VITA 65.0, Section 5.1.8.

T2-RUL-0165: 3U Payload Profile 2 Modules containing backplane USB interfaces called out in ANSI/VITA 65.1 MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15 **shall** populate pins for the USB interface(s) in accordance with the USB usage defined in ANSI/VITA 65.0 Table 14.2.16-2.

T2-RUL-0166: 3U Payload Profile 2 Modules containing backplane SATA (Serial Advanced Technology Attachment) interfaces called out in ANSI/VITA 65.1 MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15 **shall** populate pins for the SATA interface in accordance with the SATA usage defined in ANSI/VITA 65.0 Table 14.2.16-2.

T2-RUL-0167: 3U Payload Profile 2 Modules containing backplane DisplayPort interfaces called out in ANSI/VITA 65.1 MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15 **shall** populate pins for the DisplayPort interface(s) in accordance with the DisplayPort usage defined in ANSI/VITA 65.0 Table 14.2.16-2.

5.1.1.1.2.3.3 3U Payload Profile 3: PAY-1F1U1S1S1U1U4F1J

T2-RUL-0023: 3U Payload Profile 3 Modules **shall** conform to the Slot Profiles SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-n per ANSI/VITA 65.0, Section 14.6.13.

T2-RUL-0103: 3U Payload Profile 3 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-0

T2-RUL-0024: 3U Payload Profile 3 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-1F1U1S1S1U1U4F1J-16.6.13-1

5.1.1.1.2.3.4 3U Payload Profile 4: PAY-1F1U1S1S1U1U2F1H

T2-RUL-0104: 3U Payload Profile 4 Modules **shall** conform to the Slot Profiles SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n per ANSI/VITA 65.0, Section 14.6.11.

T2-RUL-0042: 3U Payload Profile 4 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0
- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-1
- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-2
- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-4

T2-RUL-0043: 3U Payload Profile 4 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-1
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-2
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-3
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-4
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-5
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-6
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-9
- MOD3-PAY-1F1U1S1S1U1U2F1H-16.6.11-10

5.1.1.1.2.3.5 3U Payload Profile 5: PAY-1F1F2U1TU1T1U1T

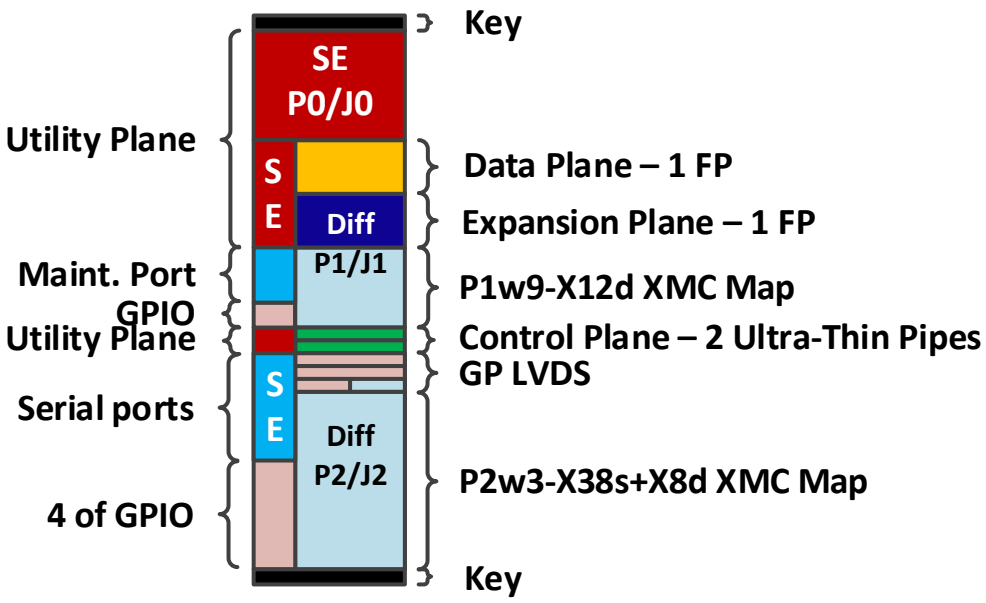
T2-RUL-0068: 3U Payload Profile 5 Modules **shall** conform to the Slot Profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16 per ANSI/VITA 65.0, Section 14.2.16.

T2-RUL-0075: 3U Payload Profile 5 Modules **shall** conform to ANSI/VITA 46.9 XMC mapping P1w9-X12d+P2w9-X16s+X8d.

T2-RUL-0069: 3U Payload Profile 5 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-1
- MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2
- MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-3
- MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-4

5.1.1.1.2.3.6 3U Payload Profile 6: PAY-1F1F2U5S-HOST



T2-RUL-4000: The Utility Plane pins on P0/J0 **shall** be implemented as described in Table 3.7-1 and Table 3.7-2 of ANSI/VITA 65.0.

T2-RUL-4001: The single-ended Utility Plane pins on P1/J1 **shall** be implemented as described in Table 3.7-3 and Table 3.7-4 of ANSI/VITA 65.0.

T2-RUL-4002: There **shall** be pins allocated for one Maintenance Port on P1/J1, MP01, as given in TABLE 5-1, with usage complying with ANSI/VITA 65.0, Section 5.13.

T2-RUL-4003: There **shall** be a pin allocated for GPIO on P1/J1, GPIO1, as given in TABLE 5-1, with usage complying with ANSI/VITA 65.0, Section 5.15.1.

T2-RUL-4004: The Data Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document, with usage complying with ANSI/VITA 65.0, Section 6.2.2.

T2-RUL-4005: The Expansion Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document, with usage complying with ANSI/VITA 65.0, Section 6.2.2.

T2-RUL-4006: The Control Plane pins on P1/J1 **shall** be implemented as described in TABLE 5-1 of this document, with usage complying with ANSI/VITA 65.0, Section 6.2.2.

T2-RUL-4007: There **shall** be pins allocated for Serial Port on P2/J2, SER01, as given in TABLE 5-2, with usage complying with ANSI/VITA 65.0, Section 5.13.

T2-RUL-4008: There **shall** be pins allocated for an XMC mapping P1w9-X12d+P2w3-X38s+X8d as given in TABLE 5-1 and TABLE 5-2, with usage complying with ANSI/VITA 46.9, Section 4.6.

T2-RUL-4009: There **shall** be pins allocated for GPIO on P2/J2, GPIO2-GPIO5, as given in TABLE 5-2, with usage complying with ANSI/VITA 65.0, Section 5.15.1.

T2-RUL-4010: There **shall** be pins allocated for GPLVDS on P2/J2 as given in TABLE 5-2 with usage complying with ANSI/VITA 65.0, Section 5.15.2.

T2-RUL-4011: 3U Payload Profile 6 Modules **shall** conform to one of the following Module Profiles listed in TABLE **5-3.**

Table 5-1 P1/J1 Pin Mapping for PAY-1F1F2U5S-HOST

Plug-in module P1			Row G	Row F	Row E		Row D	Row C	Row B		Row A
					Even	Odd			Even	Odd	
Bplane J1			Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	DP Port 1	x4 / 2x2 / 4x1	GDiscrete1	GND	*GND-J1*	DP01-TD0-	DP01-TD0+	GND	*GND-J1*	DP01-RD0-	DP01-RD0+
2			GND	DP01-TD1-	DP01-TD1+	*GND-J1*	GND	DP01-RD1-	DP01-RD1+	*GND-J1*	GND
3			P1-VBAT	GND	*GND-J1*	DP01-TD2-	DP01-TD2+	GND	*GND-J1*	DP01-RD2-	DP01-RD2+
4			GND	DP01-TD3-	DP01-TD3+	*GND-J1*	GND	DP01-RD3-	DP01-RD3+	*GND-J1*	GND
5	EP Port 1	x4 / 2x2 / 4x1	SYS_CON*	GND	*GND-J1*	EP01-TD0-	EP01-TD0+	GND	*GND-J1*	EP01-RD0-	EP01-RD0+
6			GND	EP01-TD1-	EP01-TD1+	*GND-J1*	GND	EP01-RD1-	EP01-RD1+	*GND-J1*	GND
7			Reserved	GND	*GND-J1*	EP01-TD2-	EP01-TD2+	GND	*GND-J1*	EP01-RD2-	EP01-RD2+
8			GND	EP01-TD3-	EP01-TD3+	*GND-J1*	GND	EP01-RD3-	EP01-RD3+	*GND-J1*	GND
9	X12d XMC Map		MP01-TD	GND	*GND-J1*	Jn6-A5	Jn6-B5	GND	*GND-J1*	Jn6-D5	Jn6-E5
10			GND	Jn6-A7	Jn6-B7	*GND-J1*	GND	Jn6-D7	Jn6-E7	*GND-J1*	GND
11			MP01-RD	GND	*GND-J1*	Jn6-A9	Jn6-B9	GND	*GND-J1*	Jn6-D9	Jn6-E9
12			GND	Jn6-A15	Jn6-B15	*GND-J1*	GND	Jn6-D15	Jn6-E15	*GND-J1*	GND
13			GPIO1	GND	*GND-J1*	Jn6-A17	Jn6-B17	GND	*GND-J1*	Jn6-D17	Jn6-E17
14			GND	Jn6-A19	Jn6-B19	*GND-J1*	GND	Jn6-D19	Jn6-E19	*GND-J1*	GND
15	Control Plane		Maskable Reset*	GND	*GND-J1*	CPutp02-TD-	CPutp02-TD+	GND	*GND-J1*	CPutp02-RD-	CPutp02-RD+
16			GND	CPutp01-TD-	CPutp01-TD+	*GND-J1*	GND	CPutp01-RD-	CPutp01-RD+	*GND-J1*	GND

Table 5-2 P2/J2 Pin Mapping for PAY-1F1F2U5S-HOST

Plug-In Mod P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	GP LVDS	SER01-TX-	GND	*GND-J2*	GPlvds01-	GPlvds01+	GND	*GND-J2*	GPlvds02-	GPlvds02+
2	GP LVDS	GND	GPlvds03-	GPlvds03+	*GND-J2*	GND	GPlvds04-	GPlvds04+	*GND-J2*	GND
3	GP LVDS	SER01-TX+	GND	*GND-J2*	GPlvds05-	GPlvds05+	GND	*GND-J2*	Jn6-C1	Jn6-F1
4	X38s XMC map	GND	Jn6-C2	Jn6-C3	*GND-J2*	GND	Jn6-F2	Jn6-F3	*GND-J2*	GND
5	X38s XMC map	SER01-RX-	GND	*GND-J2*	Jn6-C4	Jn6-C5	GND	*GND-J2*	Jn6-F4	Jn6-F5
6	X38s XMC map	GND	Jn6-C6	Jn6-C7	*GND-J2*	GND	Jn6-F6	Jn6-F7	*GND-J2*	GND
7	X38s XMC map	SER01-RX+	GND	*GND-J2*	Jn6-C8	Jn6-C9	GND	*GND-J2*	Jn6-F8	Jn6-F9
8	X38s XMC map	GND	Jn6-C10	Jn6-C11	*GND-J2*	GND	Jn6-F10	Jn6-F11	*GND-J2*	GND
9	X38s XMC map	GPIO2	GND	*GND-J2*	Jn6-C12	Jn6-C13	GND	*GND-J2*	Jn6-F12	Jn6-F13
10	X38s XMC map	GND	Jn6-C14	Jn6-C15	*GND-J2*	GND	Jn6-F14	Jn6-F15	*GND-J2*	GND
11	X38s XMC map	GPIO3	GND	*GND-J2*	Jn6-C16	Jn6-C17	GND	*GND-J2*	Jn6-F16	Jn6-F17
12	X38s XMC map	GND	Jn6-C18	Jn6-C19	*GND-J2*	GND	Jn6-F18	Jn6-F19	*GND-J2*	GND
13	X8d XMC map	GPIO4	GND	*GND-J2*	Jn6-A1	Jn6-B1	GND	*GND-J2*	Jn6-D1	Jn6-E1
14	X8d XMC map	GND	Jn6-A3	Jn6-B3	*GND-J2*	GND	Jn6-D3	Jn6-E3	*GND-J2*	GND
15	X8d XMC map	GPIO5	GND	*GND-J2*	Jn6-A11	Jn6-B11	GND	*GND-J2*	Jn6-D11	Jn6-E11
16	X8d XMC map	GND	Jn6-A13	Jn6-B13	*GND-J2*	GND	Jn6-D13	Jn6-E13	*GND-J2*	GND

Table 5-3 **Module Profiles for PAY-1F1F2U5S-HOST**

Module Profile	Protocols for Copper Planes			Miscellaneous Protocols over copper
	Data Plane	Expansion Plane	Control Plane	
MOD3-PAY-1F1F2U5S-HOST	**DP01**	**EP01**	**CPutp01,CPutp02**	
MOD3-PAY-1F1F2U5S-HOST-1	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	
MOD3-PAY-1F1F2U5S-HOST-2	10GBASE-KX4 - per ANSI/VITA 65.0, Section 5.1.5	PCIe Gen 2 - per ANSI/VITA 65.0, Section 5.3.3.2	1000BASE-KX - per ANSI/VITA 65.0, Section 5.1.2	
MOD3-PAY-1F1F2U5S-HOST-3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	10GBase-KR - per ANSI/VITA 65.0, Section 5.1.7	
MOD3-PAY-1F1F2U5S-HOST-4	40GBase-KR4 - per ANSI/VITA Section 5.1.8	PCIe Gen 3 - per ANSI/VITA 65.0, Section 5.3.3.3	10GBase-KR - per ANSI/VITA 65.0, Section 5.1.7	

5.1.1.1.2.3.7 3U Payload Module with Mezzanine Site Requirements

T2-RUL-0148: 3U Payload Module mezzanine sites configured to exclusively support a PMC Mezzanine **shall** conform to ANSI/VITA 46.9, Section 4.1 (P64S) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

T2-RUL-0149: 3U Payload Module mezzanine sites configured to exclusively support a XMC Mezzanine **shall** conform to one of the following options regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector if not defined by the payload profile:

1. ANSI/VITA 46.9, Section 4.3, X8D+X12D.
2. ANSI/VITA 46.9, Section 4.4, X24S+X8D+X12D.
3. ANSI/VITA 46.9, Section 4.6, X12D+X38S+X8D.
4. ANSI/VITA 46.9, Section 4.8, X12D.

T2-RUL-0151: 3U Payload Module mezzanine sites configured to support both PMC and XMC Mezzanines **shall** conform to ANSI/VITA 46.9, Section 4.2 (X12D+P64S) regarding user defined pin mapping from the mezzanine site to the Payload Module Backplane connector.

5.1.1.1.2.3.8 3U HOST Payload Modules using ANSI/VITA 66.0 or ANSI/VITA 67.0 Connectors Requirements (Deprecated)

T2-PER-0054: 3U Payload Profile 1 Modules **may** replace the P2 connector with a blind mate connector compliant to ANSI/VITA 66.0 or ANSI/VITA 67.0 and their related dot standard.

T2-RUL-0152: If following T2-PER-0054, 3U Payload Modules **shall** conform to one of the following slot profiles per ANSI/VITA 65.1:

- SLT3-PAY-2F2U1J-14.6.9-n

T2-OBS-0147: For 3U Payload Profile 1 Modules with apertures HOST only defines the aperture type and location and not the specific connector. The J aperture takes ANSI/VITA 67.3 type D connector modules.

5.1.1.1.2.4 3U Radial Clock Payload Module Requirements

5.1.1.1.2.4.1 3U Radial Clock Payload Profile 1: TIM-2S1U22S1U2U1H

T2-RUL-0038: 3U Radial Clock Payload Profile 1 Modules **shall** conform to the Slot Profiles SLT3-TIM-2S1U22S1U2U1H-14.9.2-n per ANSI/VITA 65.0, Section 14.9.2.

T2-RUL-0105: 3U Radial Clock Payload Profile 1 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT-TIM-2S1U22S1U2U1H-14.9.2-0
- SLT-TIM-2S1U22S1U2U1H-14.9.2-1

T2-RUL-0039: 3U Radial Clock Payload Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3p-TIM-2S1U22S1U2U1H-16.9.2-1
- MOD3p-TIM-2S1U22S1U2U1H-16.9.2-2

T2-RUL-0123: 3U Radial Clock Payload Profile 1 Modules **shall** draw no more than 2.2 A from VBAT, per ANSI/VITA 65.0, Section 14.9.1.1.2.

T2-REC-0006: For requirements common to all Slot Profiles using VITA 66 and/or VITA 67 connectors, Designers **should** see ANSI/VITA 65.0, Section 6.4.4.

T2-RUL-0041: The P2/J2 location of this Slot Profile **shall** either be loaded with a VITA 67.3 type C Connector Module, any other Connector Module which fits in an Aperture Pattern H location, or left empty.

5.1.1.1.3 Switch Modules

When using multiple VPX Modules, it is often necessary to utilize a Switch Module to accomplish the necessary communication.

5.1.1.1.3.1 Common 6U and 3U HOST Switch Requirements

T2-PER-0062: Switch Modules **may** combine Control Plane ultra-thin pipes to create Control Plane fat pipes.

T2-OBS-0237: It may be necessary to combine 4 10GBASE-KR ultra-thin pipes to create a single 40GBASE-KR4 fat pipe.

T2-RUL-0513: When combining ultra-thin pipes to create a 40GBASE-KR4 fat pipe, a Switch Module **shall** comply with ANSI/VITA 65.0, Section 5.1.8.

T2-RUL-0514: When combining ultra-thin pipes to create a 100GBASE-KR4 fat pipe, a Switch Module **shall** comply with ANSI/VITA 65.0, Section 5.1.18.

5.1.1.1.3.2 6U Switch Module Requirements

T2-RUL-0520: 6U Switch Modules **shall** be implemented as 6U OpenVPX Switch Plug-In Modules per SECTION 5.4.2.3.

T2-REC-0018: In order to allow their use in a Standard Development Chassis, 6U conduction-cooled Switch Modules **should** be designed to require ≤150W per slot.

T2-PER-0034: 6U conduction-cooled Switch Modules **may** be designed to require >150W per slot, but these modules might not be properly powered in a Standard Development Chassis.

T2-RUL-0533: 6U Switch Modules **shall** follow ANSI/VITA 65.0, Section 12.1.2 with regard to Power Voltages and System Management.

T2-RUL-0532: 6U Switch Modules **shall** conform to one of the 6U Switch Profiles as listed in SECTION 5.1.1.1.3.2.

T2-RUL-0537: 6U Switch Modules **shall** conform to the 6U conduction-cooled requirements of ANSI/VITA 48.2.

5.1.1.1.3.2.1 6U Switch Profile 1: SWH-20U19F

T2-RUL-0540: 6U Switch Profile 1 Modules **shall** conform to the Slot Profile SLT6-SWH-20U19F-10.4.1 per ANSI/VITA 65.0, Section 10.4.1.

T2-RUL-0550: 6U Switch Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-SWH-20U19F-12.4.1-3
- MOD6-SWH-20U19F-12.4.1-5
- MOD6-SWH-20U19F-12.4.1-10
- MOD6-SWH-20U19F-12.4.1-15

T2-OBS-0238: Note that the MOD6-SWH-20U19F-12.4.1-3 switch has PCIe in the Data Plane, but this is the profile that would be used in a system that wants to utilize HOST Payload's PCIe Expansion Plane as a switched network. Due to the Expansion Plane being primarily used for adjunct modules, the OpenVPX ecosystem does not contain Expansion Plane Switch Modules.

5.1.1.1.3.2.2 6U Switch Profile 2: SWH-16U20F

T2-RUL-0560: 6U Switch Profile 2 Modules **shall** conform to the Slot Profile SLT6-SWH-16U20F-10.4.2 per ANSI/VITA 65.0, Section 10.4.2.

T2-RUL-0570: 6U Switch Profile 2 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-SWH-16U20F-12.4.2-3
- MOD6-SWH-16U20F-12.4.2-5

- MOD6-SWH-16U20F-12.4.2-11
- MOD6-SWH-16U20F-12.4.2-15

T2-OBS-0239: Note that the MOD6-SWH-16U20F-12.4.2-3 switch has PCIe in the Data Plane. This is the profile that would be used in a system that wants to utilize HOST Payload's PCIe Expansion Plane as a switched network. Due to the Expansion Plane being primarily used for adjunct Modules, the OpenVPX ecosystem does not contain Expansion Plane Switch Modules.

5.1.1.1.3.2.3 6U Switch Profile 3: SWH-14F16U1U15U1J

T2-RUL-0106: 6U Switch Profiles 3 Modules **shall** conform to the Slot Profiles SLT6-SWH-14F16U1U15U1J-10.8.1-n per ANSI/VITA 65.0, Section 10.8.1.

T2-RUL-0025: 6U Switch Profile 3 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT6-SWH-14F16U1U15U1J-10.8.1-0

T2-RUL-0026: 6U Switch Profile 3 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-SWH-14F16U1U15U1J-12.8.1-1
- MOD6-SWH-14F16U1U15U1J-12.8.1-2

5.1.1.1.3.3 3U Switch Module Requirements

T2-RUL-0568: 3U Switch Modules **shall** be implemented as 3U OpenVPX Switch Plug-In Modules per SECTION 5.4.2.3.

T2-REC-0019: In order to allow their use in a Standard Development Chassis, 3U conduction-cooled Switch Modules **should** be designed to require ≤75W per slot.

T2-PER-0035: 3U conduction-cooled Switch Modules **may** be designed to require >75W per slot, but these modules might not be properly powered in a Standard Development Chassis.

T2-RUL-0571: 3U Switch Modules **shall** follow ANSI/VITA 65.0, Section 16.1.2 with regard to Power Voltages and System Management.

T2-RUL-0572: 3U Switch Modules **shall** conform to one of the 3U Switch Profiles as listed in SECTION 5.1.1.1.3.3.

T2-RUL-0587: 3U Switch Modules **shall** conform to the 3U conduction-cooled requirements of ANSI/VITA 48.2.

5.1.1.1.3.3.1 3U Switch Profile 1: SWH-6F8U

T2-RUL-0573: 3U Switch Profile 1 Modules **shall** conform to the Slot Profile SLT3-SWH-6F8U-14.4.15 per ANSI/VITA 65.0, Section 14.4.15.

T2-RUL-0045: If a 3U Switch Profile 1 Module implements the Control Plane thin pipe, a Switch Module **shall** use the Control Plane thin pipe exclusively as part of the SIOTI.

T2-RUL-0575: 3U Switch Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-SWH-6F8U-16.4.16-1
- MOD3-SWH-6F8U-16.4.16-2

5.1.1.1.3.3.2 3U Switch Profile 2: SWH-2F24U

T2-RUL-0576: 3U Switch Profile 2 Modules **shall** conform to the Slot Profile SLT3-SWH-2F24U-14.4.3 per ANSI/VITA 65.0, Section 14.4.3.

T2-PER-0101: If an application requires more than 24 Ultra-Thin Pipes the P1 Fat Pipes of 3U Switch Profile 2 **may** be repartitioned into Ultra-Thin Pipes.

T2-RUL-0591: If only one of the two available Fat Pipes on P1 of the 3U Switch Profile 2 is repartitioned it **shall** be the Fat Pipe closer to P2.

T2-PER-0021: If more than 2 Fat-Pipes are needed, the UTPs, CPutp01 thru CPutp24, **may** be repartitioned into Fat Pipes.

T2-RUL-0581: 3U Switch Profile 2 Modules **shall** conform to MOD3-SWH-2F24U-16.4.3-4 per TABLE 5-4.

Table 5-4 3U 2F24U Switch Module Profile

Module Profile	Slot Profile	CPutp01-CPutp24	CP01, CP02(FP)	Comments
MOD3-SWH-2F24U-16.4.3-4	SLT3-SWH-2F24U-14.4.3	10GBASE-KR -- 5.1.7, 40GBASE-KR4 -- 5.1.8	40GBASE-KR4 -- 5.1.8, 10GBASE-KR -- 5.1.7	Each port can be configured separately for 4 lanes of 10GBASE-KR or a single 40GBASE-KR4.

Note: Sections in TABLE 5-4 reference ANSI/VITA 65.0.

5.1.1.1.3.3.3 3U Switch Profile 3: SWH-6F1U7U

T2-RUL-0081: 3U Switch Profile 3 Modules **shall** conform to the Slot Profile SLT3-SWH-6F1U7U-14.4.14 per ANSI/VITA 65.0, Section 14.4.14.

T2-RUL-0082: 3U Switch Profile 3 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-SWH-6F1U7U-16.4.15-1
- MOD3-SWH-6F1U7U-16.4.15-2

5.1.1.1.3.3.4 3U Switch Profile 4: SWH-4F1U7U1J

T2-RUL-0107: 3U Switch Profile 4 Modules **shall** conform to the Slot Profiles SLT3-SWH-4F1U7U1J-14.8.7-n per ANSI/VITA 65.0, Section 14.8.7.

T2-RUL-0013: 3U Switch Profile 4 Modules **shall** conform one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT3-SWH-4F1U7U1J-14.8.7-0
- SLT3-SWH-4F1U7U1J-14.8.7-1

T2-RUL-0014: 3U Switch Profile 4 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.0 and ANSI/VITA 65.1:

- MOD3-SWH-4F1U7U1J-16.8.7-1
- MOD3-SWH-4F1U7U1J-16.8.7-2

5.1.1.1.3.3.5 3U Switch Profile 5: SWH-1F1S1S1U1U1K

T2-RUL-0111: 3U Switch Profile 5 Modules **shall** conform to the Slot Profiles SLT3-SWH-1F1S1S1U1U1K-14.8.8-n per ANSI/VITA 65.0, Section 14.8.8.

T2-RUL-0112: 3U Switch Profile 5 Modules **shall** conform to one of the following Slot Profiles per ANSI/VITA 65.1:

- SLT3-SWH-1F1S1S1U1U1K-14.8.8-0
- SLT3-SWH-1F1S1S1U1U1K-14.8.8-1

T2-RUL-0113: 3U Switch Profile 5 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-SWH-1F1S1S1U1U1K-16.8.8-1
- MOD3-SWH-1F1S1S1U1U1K-16.8.8-2

5.1.1.1.4 External I/O Modules

External I/O Modules are meant to only be used as dedicated I/O modules acting as interfaces between platform-specific I/O over the User Defined (UD) pins and processing modules over the SCTI, i.e. PCIe or Ethernet communication. These profiles maximize the number of UD pins to enable the module to interface with a maximum quantity of platform I/O.

Due to having to interface with I/O, these Modules will most likely have I/O and some data processing; however, External I/O Modules are not meant to be used as the main processing resources, such as a Single Board Computer or computing intensive Data Processors. This is true even though both the 4U2U and the 2U2U are technically Payload Modules in ANSI/VITA 65.0. The purpose of these modules are to allow a system designer to have a central hub for all platform specific I/O and thus only use standardized signals on modules within the system.

5.1.1.1.4.1 Common 6U and 3U External I/O Module Requirements

T2-PER-0092: The User Defined pins on External I/O Modules **may** be connected to other External I/O Modules or HOST Mezzanine Modules.

T2-OBS-0074: Instead of routing platform specific I/O to non-standard payloads, integrators can utilize an External I/O Module as the platform I/O "data-center" where, a single module (or multiple if required) can interface with the platform over platform specific connections and the rest of the payload modules over standard Expansion or Data Plane interfaces.

5.1.1.1.4.2 6U External I/O Module Requirements

T2-RUL-0064: 6U External I/O Modules **shall** conform to the 6U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0065: 6U External I/O Modules **shall** follow ANSI/VITA 65.0, Section 12.1.2 with regards to Power Voltages and System Management.

T2-OBS-0042: Refer to ANSI/VITA 65.0, Recommendation 12.1.1.2-1 regarding maximum module power draw.

T2-RUL-0066: 6U External Modules **shall** conform to one of the 6U External I/O Profiles as listed in SECTION 5.1.1.1.4.2.

5.1.1.1.4.2.1 6U External I/O Profile 1: PAY-4U2U

T2-RUL-0027: 6U External I/O Profile 1 Modules **shall** conform to the Slot Profile SLT6-PAY-4U2U-10.2.8 per ANSI/VITA 65.0, Section 10.2.8.

T2-RUL-0028: 6U External I/O Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD6-PAY-4U2U-12.2.8-1
- MOD6-PAY-4U2U-12.2.8-2

5.1.1.1.4.2.2 6U External I/O Profile 2: PER-2F

T2-RUL-0067: 6U External I/O Profile 2 Modules **shall** conform to the Slot Profile SLT6-PER-2F-10.3.2 per ANSI/VITA 65.0, Section 10.3.2.

T2-RUL-0072: 6U External I/O Profile 2 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

MOD6-PER-2F-12.3.2-2

5.1.1.1.4.3 3U External I/O Module Requirements

T2-RUL-0073: 3U External I/O Modules **shall** conform to the 3U conduction-cooled requirements of ANSI/VITA 48.2.

T2-RUL-0074: 3U External I/O Modules **shall** follow ANSI/VITA 65.0, Section 16.1.2 with regards to Power Voltages and System Management.

T2-OBS-0043: Refer to ANSI/VITA 65.0, Recommendation 16.1.1.2-1 regarding maximum module power draw.

T2-RUL-0078: 3U External Modules **shall** conform to one of the 3U External I/O Profiles as listed in SECTION 5.1.1.1.4.3.

5.1.1.1.4.3.1 3U External I/O Profile 1: PAY-2U2U

T2-RUL-0015: 3U External I/O Profile 1 Modules **shall** conform to the Slot Profile SLT3-PAY-2U2U-14.2.17 per ANSI/VITA 65.0, Section 14.2.17.

T2-RUL-0022: 3U External I/O Profile 1 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PAY-2U2U-16.2.16-1
- MOD3-PAY-2U2U-16.2.16-2

5.1.1.1.4.3.2 3U External I/O Profile 2: PER-1U

T2-RUL-0292: 3U External I/O Profile 2 Modules **shall** conform to the Slot Profile SLT3-PER-1U-14.3.3 per ANSI/VITA 65.0, Section 14.3.3.

T2-RUL-0293: 3U External I/O Profile 2 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PER-1U-16.3.3-2
- MOD3-PER-1U-16.3.3-3

5.1.1.1.4.3.3 3U External I/O Profile 3: PER-1F

T2-RUL-0076: 3U External I/O Profile 3 Modules **shall** conform to the Slot Profile SLT3-PER-1F-14.3.2 per ANSI/VITA 65.0, Section 14.3.2.

T2-RUL-0077: 3U External I/O Profile 3 Modules **shall** conform to one of the following Module Profiles per ANSI/VITA 65.1:

- MOD3-PER-1F-16.3.2-2
- MOD3-PER-1F-16.3.2-3

5.1.1.2 Power Supply Modules

5.1.1.2.1 Common 6U and 3U Power Supply Module Requirements

T2-RUL-0310: PSM requirements **shall** be applied using the following order of precedence:

1. Requirements of SECTION 5.1.1.2.2 6U Power Supply Module Requirements and SECTION 5.1.1.2.3 3U Power Supply Module Requirements
2. Requirements of SECTION 5.1.1.2.1 Common 6U and 3U Power Supply Module Requirements
3. Requirements of ANSI/VITA 62.0

T2-OBS-0170: PSMs can be configured as a single-stage or two-stage power supply system as specified by ANSI/VITA 62.0, Section 1.2.

T2-OBS-0180: PSMs can utilize energy storage modules as specified by ANSI/VITA 62.0 to satisfy Target System power hold-up requirements.

T2-RUL-0320: PSMs **shall** assert the FAIL* signal when PO1, PO2, PO3, or AUX voltages are not within their voltage specifications per ANSI/VITA 62.0, Recommendation 3.3-2.

T2-RUL-0330: PSMs that accept external prime input power **shall** do so in accordance with ANSI/VITA 62.0, Section 6.5.1.

T2-OBS-0190: PSMs that accept external prime input power include Single-Stage Power Subsystem Modules and Front-End Modules of Two-Stage Power Subsystems.

T2-RUL-0340: PSMs that supply power to the HOST VPX slot portion of the HOST Backplane **shall** output +12V final power in accordance with ANSI/VITA 62.0, Section 4.6.1.2 and Section 4.6.1.1.1.

T2-RUL-0350: PSMs that supply power to the HOST VPX slot portion of the HOST Backplane **shall** output +5V final power in accordance with ANSI/VITA 62.0, Section 4.6.1.5.

T2-RUL-0360: PSMs that supply power to the HOST VPX slot portion of the HOST Backplane **shall** output 3.3V_AUX in accordance with ANSI/VITA 62.0, Section 4.6.1.7.

T2-RUL-0370: PSMs that supply power to the HOST VPX slot portion of the HOST Backplane **shall** output +/-12V AUX in accordance with ANSI/VITA 62.0, Section 4.6.1.8.

T2-OBS-0200: PSMs supplying power to HOST VPX Modules include Single-Stage Power Subsystem Modules and Back-End Modules of a Two-Stage Power Subsystem.

T2-OBS-0210: The ANSI/VITA 62.0 requirements for +48V final power are not applicable to this Tier 2 Core Technology Standard.

T2-RUL-0371: PSMs **shall** have the chassis pin connected to their front panel and covers.

T2-RUL-0372: PSMs **shall** have the chassis pin isolated from the SIGNAL_RETURN pin.

T2-RUL-0373: PSMs **shall** have the chassis pin isolated from power returns, such as the POWER_RETURN pins.

T2-RUL-0374: PSMs **shall** have the chassis pin isolated from the -DC_IN/ACN pin.

T2-OBS-0205: The rules for isolating the chassis pins come from ANSI/VITA 62.0, Recommendations in Section 4.7.

T2-RUL-0380: PSMs outputting an intermediate power **shall** explicitly define the nominal voltage level for the intermediate power.

T2-RUL-0390: PSMs having intermediate power as an input **shall** explicitly define the nominal voltage level for the intermediate power.

T2-OBS-0220: The SPDI is implemented using the OpenVPX Utility Plane as well as additional requirements specified herein.

T2-OBS-0230: PSMs make use of a subsection of the CMTI OpenVPX Utility Plane since they do not contain traditional processing elements.

T2-RUL-0391: PSMs **shall** conform to the requirements of ANSI/VITA 62.0 except where specified herein.

5.1.1.2.1.1 Common Energy Storage Module Requirements

T2-RUL-0480: Energy Storage Modules **shall** accept an input of the intermediate voltage in accordance with ANSI/VITA 62.0, Section 4.5.

T2-RUL-0490: Energy Storage Modules **shall** output the intermediate voltage in accordance with ANSI/VITA 62.0, Section 4.5.

5.1.1.2.2 6U Power Supply Module Requirements

T2-RUL-0300: 6U PSMs **shall** conform to the mechanical requirements of ANSI/VITA 48.2 for 6U conduction cooled modules except where specified herein.

5.1.1.2.2.1 6U Front-End Module Requirements

T2-OBS-0231: Requirements related to Front-End Modules are in ANSI/VITA 62.0, Section 4.6.2.1.2.

5.1.1.2.2.2 6U Back-End Module Requirements

T2-OBS-0232: Information and Requirements related to input of intermediate voltage are in ANSI/VITA 62.0, Section 4.6.2.2 and 6.5.1.

5.1.1.2.2.3 6U Single-Stage Module Requirements

T2-RUL-0500: 6U Single-Stage Modules **shall** route the intermediate voltage to the ANSI/VITA 62.0 pins labeled “POS_FILT_OUT” and “NEG_FILT_OUT” in accordance with ANSI/VITA 62.0, Section 6.5.2.

5.1.1.2.3 3U Power Supply Module Requirements

T2-RUL-0502: 3U PSMs **shall** conform to the mechanical requirements of ANSI/VITA 48.2 for 3U conduction cooled modules except where specified herein.

T2-RUL-0503: 3U PSMs that supply power to the HOST VPX slot portion of the Backplane **shall** output +3.3V final power in accordance with ANSI/VITA 62.0, Section 4.6.1.4.

5.1.1.2.3.1 3U Front-End Module Requirements

T2-OBS-0233: Requirements related to Front-End Modules are in ANSI/VITA 62.0, Section 4.6.2.1.1.

5.1.1.2.3.2 3U Back-End Module Requirements

T2-OBS-0234: Information and Requirements related to input of intermediate voltage are in ANSI/VITA 62.0, Section 4.6.2.1 and Section 5.5.1.

5.1.2 Mezzanine Requirements

5.1.2.1 Common Mezzanine Requirements

HOST Mezzanine Modules are HOST Modules that mount onto a HOST Payload Module. The two types of HOST Mezzanine form factors are PMC and XMC.

T2-RUL-0590: Requirements for HOST Mezzanine Modules **shall** be applied using the following order of precedence:

1. Requirements of this HOST Tier 2 Standard (including additions or exclusions to PMC/XMC standards)
2. Mezzanine Module requirements of IEEE 1386.1 and ANSI/VITA 42.0 for PMCs and XMCs respectively

T2-RUL-0600: HOST Mezzanine Modules **shall** perform all of their required I/O functions through their mezzanine connectors.

T2-OBS-0240: Some sections of the mezzanine card standards contain requirements for mezzanine card front panel I/O. These requirements are not applicable to this Tier 2 technology. This Tier 2 technology only utilizes mezzanine card I/O that pass through the mezzanine card connector.

T2-RUL-0610: HOST Mezzanine Modules **shall** conform to the interface requirements of the SCTI for Mezzanine Modules per SECTION 5.4.1.2.

T2-OBS-0250: The SCTI for PMCs is implemented using OpenVPX high-speed serial interconnects to *Peripheral Component Interconnect* (PCI) bridging as defined in SECTION 5.4.1.2.2.

T2-OBS-0260: The CMTI for Mezzanines is implemented using the OpenVPX Utility Plane in conjunction with the appropriate mezzanine card standard defined in SECTION 5.4.1.5.

T2-OBS-0270: The SPDI for Mezzanines is implemented using the OpenVPX Utility Plane in conjunction with the appropriate mezzanine card standard defined in SECTION 5.4.1.6.

T2-PER-0070: A Mezzanine connector that has no signals routed to it **may** be left unpopulated.

T2-PER-0080: A Mezzanine connector **may** leave a user defined signal as a no connect if the signal is not implemented in the mezzanine design.

T2-REC-0011: 6U Payload Modules with only one Mezzanine site **should** use a mapping to P3 and P4.

T2-OBS-0242: By using P3 and P4 for T2-REC-0011, if optical and/or coax connections are used, P6 and possibly P5 would be used for this purpose.

5.1.2.2 XMC Mezzanine Requirements

T2-RUL-0620: XMC Mezzanines **shall** conform to the requirements of ANSI/VITA 42.0 Standard for Switched Mezzanine Cards (herein referred to as XMC).

T2-RUL-0650: XMC Mezzanines that do not require utilization of all available user I/O signals **shall** leave the remaining unused signals as no connects.

T2-REC-0012: The higher priority I/O signals of the XMC Mezzanine **should** populate pins in the following order of ANSI/VITA 46.9 patterns:

1. X12d
2. X8d
3. X24s
4. X38s

T2-OBS-0245: There will be instances where Payload Modules only route a portion of the XMC I/O to the HOST backplane connectors and by following the priority stated in T2-REC-0012, the chance that a high priority signal will not be routed to the Backplane is decreased.

5.1.2.3 PMC Mezzanine Requirements

T2-RUL-0660: PMC Mezzanines **shall** conform to the requirements of IEEE Std. 1386.1 Standard for PCI Mezzanine Cards (referred to as PMC).

T2-RUL-0690: PMC Mezzanines that do not require utilization of all available user I/O signals **shall** leave the remaining unused signals as no connects.

T2-RUL-0700: If a PMC Mezzanine is implementing a 64-bit PCI bus for PMC communication, a PMC Mezzanine **shall** populate a minimum of Pn1, Pn2, and Pn3.

T2-OBS-0243: Pn4 is an optional connector used only for User I/O in 64-bit PCI bus implementations of PMCs.

T2-RUL-0710: If a PMC Mezzanine is implementing a 32-bit PCI bus for PMC communication, a PMC Mezzanine **shall** populate a minimum of Pn1 and Pn2.

T2-OBS-0244: Pn3 and Pn4 are optional connectors used only for User I/O in 32-bit PCI bus implementations of PMCs.

5.2 Hardware System Management Option

T2-OBS-0289: SECTION 5.3 is planned to be required in a future version of this standard.

T2-RUL-0286: SM[1..0] (IPMB-A) **shall** be unconnected to any electrical components on Level B Conformant Plug-In Modules.

T2-RUL-0287: SM[3..2] (IPMB-B) **shall** be unconnected to any electrical components on Level B Conformant Plug-In Modules.

T2-PER-0086: A Plug-In Module **may** route the SM[3..0] pins to an unpopulated component.

T2-RUL-0288: Level A Conformant Plug-In Modules **shall** utilize SM[1..0] (IPMB-A) and SM[3..2] (IPMB-B).

T2-OBS-0011: Level A and Level B Conformant Modules are specified in SECTION 4.1.5.

5.3 Hardware System Management

5.3.1 Hardware System Management Overview

The Hardware System Management extends ANSI/VITA 46.11, which in turn leverages both the IPMI standard and the PICMG Advanced TCA (ATCA) 3.0 standard. HOST provides additional functional requirements to ANSI/VITA 46.11 and IPMI. Hardware System Management provides the following capabilities:

- **Sensor Management** – temperature, voltage, system modes etc.
- **System/Module Inventory** – vendor identification, model number, serial number, revision identification
- **System/Module Configuration** – parameter settings, policy settings
- **FRU Recovery** – reset a module, power cycle a module
- **Diagnostic Management** – initiate diagnostics, collect diagnostic results

HOST differentiates from ANSI/VITA 46.11 in that it provides further standardization for key interfaces, provides additional capabilities related to defense systems, and takes into consideration the perspective of defense system developers and integrators.

The following are key differentiations from ANSI/VITA 46.11:

HOST provides further standardization to:

- The payload interface
- The *Intelligent Platform Management Bus* (IPMB) speed.

5.3.2 Hardware System Management Architecture

Hardware System Management is hierarchical in nature with the System Manager at the highest level. A System Manager may communicate with the *Chassis Manager* at the subsequent level. The Chassis Manager communicates with the Intelligent Platform Management Controllers (IPMCs) at the lowest level. Consistent with 46.11, the System Manager implementation details are outside the scope of this standard. The System Manager is typically application level software which can query or command the Chassis Manager for details regarding the whole HOST Chassis; the System Manager can also query or command an individual IPMC via the Chassis Manager. The below diagram, FIGURE 5.3-1, shows additional interfaces such as the SMI and Payload Interface which are required by HOST.

For additional details in regards to the three logical layers in system management refer to ANSI/VITA 46.11, Section 1.2.3.1.

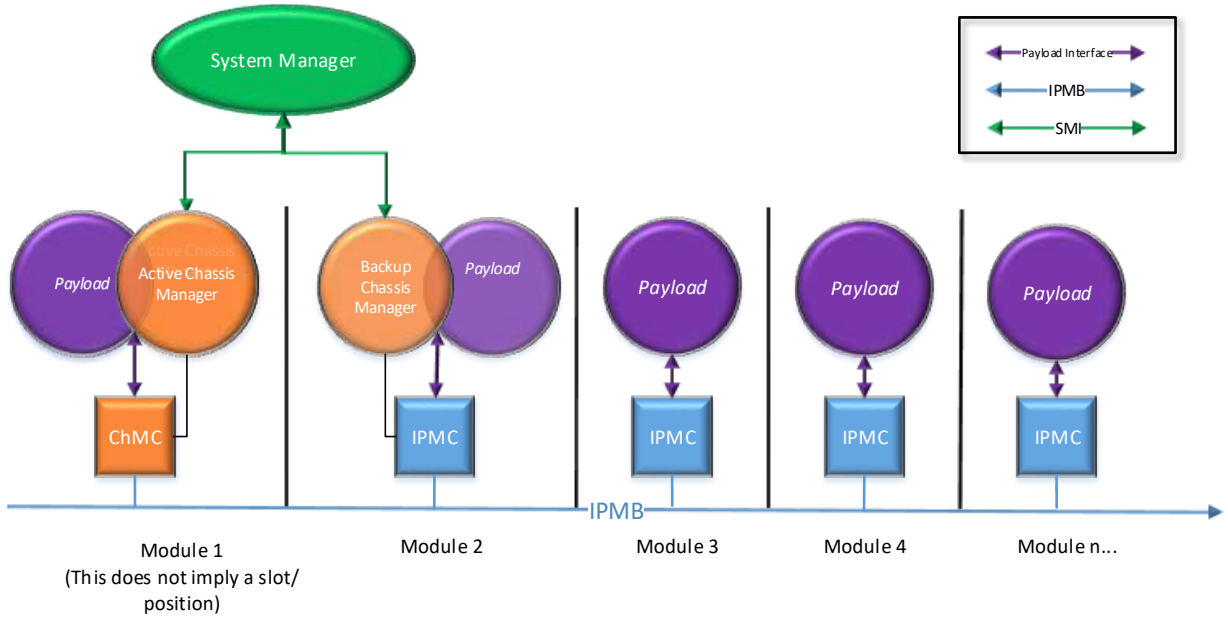


Figure 5.3-1 – Hardware System Management

5.3.3 Hardware System Management Requirements

T2-RUL-0046: HOST Plug-In Modules **shall** contain an IPMC that conforms to the requirements in SECTION 5.3.3.2, and SECTION 5.3.3.3 below.

T2-RUL-0047: HOST Chassis **shall** contain at least one Chassis Manager that conforms to the requirements in SECTION 5.3.3.1, and SECTION 5.3.3.3 below.

5.3.3.1 Chassis Manager

According to ANSI/VITA 46.11 a Chassis Manager is,

> *A logical entity in the VPX System Management architecture whose primary responsibility is to manage the IPMCs within a Chassis and provide a communication path between the System Manager and the aforementioned IPMCs. A Chassis Manager includes and can potentially be completely implemented on a Chassis Management Controller. The Chassis Manager is the middle level logical management layer in the VPX System Management architecture.*

The Chassis Manager uses its Chassis Management Controller (ChMC) to communicate with IPMCs via the IPMB utilizing the IPMI protocol. The interface between the Chassis Manager and ChMC is internal to the Chassis Manager. The Chassis Manager is not required to be physically located on a specific HOST Module or other piece of hardware within the Enclosure, but can reside anywhere as specified by the Target System requirements.

The Tier 2 HOST Standard does not require or restrict the presence of multiple *Active Chassis Managers* within an Enclosure as long as each Active Chassis Manager is connected to a separate IPMB. In this case, the Chassis Managers are considered to be in separate HOST Chassis. However, if there are *Backup*

Chassis Managers implemented on the same IPMB, only one Chassis Manager should be active at any time.

The Chassis Manager provides a point of entry for the System Manager to join in managing the HOST Chassis and interacting with the main aggregation of IPMC information.

T2-RUL-0048: Chassis Managers **shall** conform to the requirements of an ANSI/VITA 46.11 Tier-2 Chassis Manager.

T2-RUL-0720: ChMCs **shall** utilize the system management bus pins SM[1..0] (IPMB-A) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-RUL-0285: ChMCs **shall** utilize the system management bus pins SM[3..2] (IPMB-B) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-OBS-0280: The system management buses SM[3..0] represent the physical lines used for management communications. These data lines also make up a portion of the CMTI. See SECTION 5.4.1.5 for more details about the CMTI.

T2-RUL-0296: Chassis Managers **shall** support the *System Manager Interface* (SMI) over Ethernet.

T2-OBS-0061: The System Manager Interface need not be used at any time but the Chassis Manager must fully support such connection when made.

T2-RUL-0331: Chassis Managers **shall** use the same clock for all logged messages.

T2-RUL-0351: Chassis Managers **shall** use the same clock for all logged data.

T2-RUL-0352: Chassis Managers **shall** use the same clock for all logged events.

T2-OBS-0075: The IPMI command “Set SEL Time” can be used to set the local clock on the Chassis Manager.

T2-REC-0008: Coordinated Universal Time (UTC) should be used for all clocks within a system.

T2-RUL-0299: Chassis Management Controllers (ChMCs) **shall** comply with the IPMC requirements in this HOST Tier 2 Standard.

5.3.3.2 IPMCs

According to ANSI/VITA 46.11 an IPMC is,

> *The portion of a FRU that interfaces with a Chassis’ IPMB and represents the FRU and any devices subsidiary to it. The IPMC is the lowest level physical management entity in the VPX System Management architecture. This term can apply either to the physical or logical entity which performs this function (depending on context).*

The following HOST requirements enable additional capabilities including access to the Payload Interface and ultimately to the System Manager, system modes, etc.

T2-RUL-0063: IPMCs **shall** conform to the requirements of an ANSI/VITA 46.11 Tier-2 IPMC.

T2-RUL-0755: IPMCs **shall** utilize the system management buses SM[1..0] (IPMB-A) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-RUL-1106: IPMCs **shall** utilize the system management buses SM[3..2] (IPMB-B) as defined by ANSI/VITA 65.0, Section 3.4.5, System Management Buses.

T2-OBS-0290: The SYSRESET* requirements of ANSI/VITA 46.11, Section 4.1.9 supersede the requirements of ANSI/VITA 65.0.

T2-RUL-0821: IPMCs **shall** implement, in either volatile or non-volatile memory, a System Event Log as defined in IPMI, Section 31 “System Event Log (SEL) Commands” and Section 32 “SEL Record Formats.”

T2-RUL-0337: IPMCs **shall** use the same clock for all logged messages.

T2-RUL-0353: IPMCs **shall** use the same clock for all logged data.

T2-RUL-0354: IPMCs **shall** use the same clock for all logged events.

T2-OBS-0076: The IPMI command “Set SEL Time” can be used to set the local clock on the IPMC.

T2-OBS-0291: Per ANSI/VITA 46.11 Rule 9.2.2-1 and Rule 9.2.2-2 and Parameter M0_P1 in Table 9.2.2-1, IPMCs are required to receive messages sent with clock frequencies between 100 kHz and 400 kHz on SCL.

T2-RUL-1107: IPMCs **shall** have a user-accessible configuration parameter to select between driving the IPMB-A and IPMB-B clock, SCL, at 100 kHz or 400 kHz, when sending a message.

T2-REC-0052: IPMCs **should** have accessible methods for updating configuration parameters to allow for different system requirements.

5.3.3.3 Additional Mandatory Messages

TABLE 5-5 represents the additional IPMI formatted messages mandated by HOST. HOST standardizes interfaces including Chassis Manager-IPMB, IPMC-IPMB, IPMC-Payload Interface, Chassis Manager-Payload Interface, and the Chassis Manager-System Manager Interface. All other messages not required by this HOST Standard or an ANSI/VITA 46.11 Tier-2 IPMC or Chassis Manager are optional.

T2-RUL-0332: Chassis Managers **shall** implement all the messages listed in TABLE 5-5 that are designated as mandatory for the Chassis Manager-IPMB interface.

T2-OBS-0036: The messages listed in Table 5-5 are in addition to the required messages of a Tier-2 Chassis Manager in ANSI/VITA 46.11.

T2-RUL-0333: Chassis Managers **shall** make all supported IPMI commands and data accessible through the System Manager Interface.

T2-RUL-0335: ChMCs for payload-resident Chassis Managers **shall** make all supported IPMI commands and data accessible through the Payload Interface.

T2-OBS-0071: Requiring ChMCs to make all supported IPMI commands accessible through the Payload Interface for payload-resident Chassis Managers is consistent with ANSI/VITA 46.11 Rule 4.1.3-3, which requires a payload-resident Chassis Manager and ChMC utilize the Payload Interface for Rule 4.1.3-3’s specified message set.

T2-RUL-0282: ChMCs for payload-resident Chassis Managers **shall** have an ANSI/VITA 46.11 Payload Interface accessible to the payload.

T2-REC-0283: Integrators **should** provide the hardware specification for the Payload Interface chosen on Chassis Managers, ChMCs, and IPMCs in the HOST Tier 3 specification.

T2-RUL-0336: Chassis Managers **shall** implement only IPMI formatted messages over the IPMB and SMI.

T2-OBS-0037: The requirement that Chassis Managers only implement IPMI formatted messages does not prevent the use of OEM defined messages over the IPMB and SMI as long as they use the OEM network functions as defined in the IPMI specification.

T2-PER-0082: Chassis Managers **may** implement additional IPMI formatted messages than what is required by an ANSI/VITA 46.11 Tier-2 Chassis Manager and what is defined in TABLE 5-5.

T2-PER-0085: Chassis Managers **may** be exempted from transmitting messages based on superseding Platform requirements.

T2-OBS-0296: Superseding Platform requirements could include classified requirements, security guidelines, safety considerations, laws, regulations, or any other higher precedence requirements as defined by the program.

T2-RUL-0338: IPMCs **shall** implement all the messages listed in TABLE 5-5 that are designated as mandatory for the IPMC-IPMB interface.

T2-OBS-0038: The messages listed in Table 5-5 are in addition to the required messages of a Tier-2 IPMC in ANSI/VITA 46.11.

T2-RUL-0284: If an IPMC is connected to a processing unit, the IPMC **shall** make all supported IPMI commands and data accessible through an ANSI/VITA 46.11 Payload Interface.

T2-REC-0007: IPMCs on a HOST Payload Module **should** implement a Payload Interface accessible to the payload.

T2-REC-0272: Integrators **should** provide the hardware specification for the Payload Interface chosen on Chassis Managers and IPMCs in the HOST Tier 3 specification.

T2-RUL-0339: IPMCs **shall** implement only IPMI formatted messages over the Payload Interface and the IPMB.

T2-OBS-0039: The requirement that IPMCs only implement IPMI formatted messages does not prevent the use of OEM defined messages as long as they use the OEM network functions as defined in the IPMI specification.

T2-PER-0083: IPMCs **may** implement additional IPMI formatted messages than what is defined in TABLE 5-5.

T2-OBS-0072: The rules of this section are requirements on hardware to include and support Hardware System Management messages, but it is left to the discretion of an integrator to determine when the use of a message is appropriate for each system. For example, an integrator can choose to utilize event generation or not.

T2-PER-0084: From ANSI/VITA 46.11, the Payload Test Results Sensor Event Message Bytes 6 (Event Data 2) & 7 (Event Data 3) data **may** be used to provide additional supporting data.

T2-REC-0044: Integrators **should** provide all related information in regards to OEM (Original Equipment Manufacturer) defined information such as OEM codes to the applicable program management office for interoperability purposes.

Table 5-5 Additional Mandatory Messages

Message Name	Standard section	IPMC - IPMB	CHMGR - IPMB
FRU Control	VITA 46.11, Section 10.1.3.6	M	AV 46.11 M
Set FRU State Policy BITs	VITA 46.11, Section 10.1.3.9	M	AV 46.11 M
Get FRU State Policy BITS	VITA 46.11, Section 10.1.3.8	M	AV 46.11 M
Get Mandatory Sensor Numbers	VITA 46.11, Section 10.1.3.26	M	M
Get SEL Info	IPMI V2.0, Section 31.2	M	AV 46.11 M
Get SEL Entry	IPMI V2.0, Section 31.5	M	AV 46.11 M
Get SEL Time	IPMI V2.0, Section 31.10	M	AV 46.11 M
Set SEL Time	IPMI V2.0, Section 31.11	M	AV 46.11 M
Set FRU Activation	VITA 46.11 Section 10.1.3.10	M	AV 46.11 M

Note: CHMGR = Chassis Manager, AV 46.11 M = Already mandatory in ANSI/VITA 46.11

5.4 Hardware

HOST standardizes hardware components so that each HOST Component, as defined in SECTION 5.4.2, can interface with another HOST Component. The different hardware components that are standardized

are the Modules, Transmission Interfaces routed between Modules, and Enclosures. The HOST Components section contains the Form Factor and other mechanically oriented requirements for different hardware components, while the sections preceding it contain the electrically oriented requirements for different hardware components.

5.4.1 HOST Transmission Interfaces

The HOST Architecture establishes five Transmission Interfaces that facilitate logical and physical connectivity within the system. Each Transmission Interface, except for the SIOTI and *External I/O Transmission Interface* (EIOTI), contains elements of one or more planes defined in the ANSI/VITA 65.0 multi-plane architecture. This Tier 2 Core Technology Standard defines how the ANSI/VITA 65.0 multi-plane architecture is applied to the HOST Transmission Interfaces in 6U and 3U systems. These Interfaces are:

- **System Communications** - The SCTI utilizes the Data Plane, the portions of the Control Plane not using BASE-T Ethernet, and the Expansion Plane.
- **Chassis Management** - The CMTI utilizes the ANSI/VITA 65.0 Utility Plane with the additional requirements of ANSI/VITA 46.11 for management communications. The ANSI/VITA 65.0 Control Plane may also be utilized for chassis management communications.
- **System I/O** - The SIOTI is an I/O routing layer that primarily utilizes the ANSI/VITA 65.0 User Defined I/O. The VPX Module Thin-Pipes are also part of the SIOTI.
- **External I/O** - The EIOTI for this HOST Tier 2 Core Technology Standard includes the connectors used to bring the system I/O signals off the HOST Backplane, the connectors located on a front or rear panel, and any cables, connectors, and/or circuitry in between.
- **System Power Distribution** - The SPDI will use the power distribution portions of the ANSI/VITA 46.0 and ANSI/VITA 65.0 Utility Plane with input/output power interfaces as defined by ANSI/VITA 62.0 for modular power supplies and the requirements of the EIOTI contained in this document.

The HOST Tier 2 Transmission Interface configuration is shown in FIGURE 5.4-1.

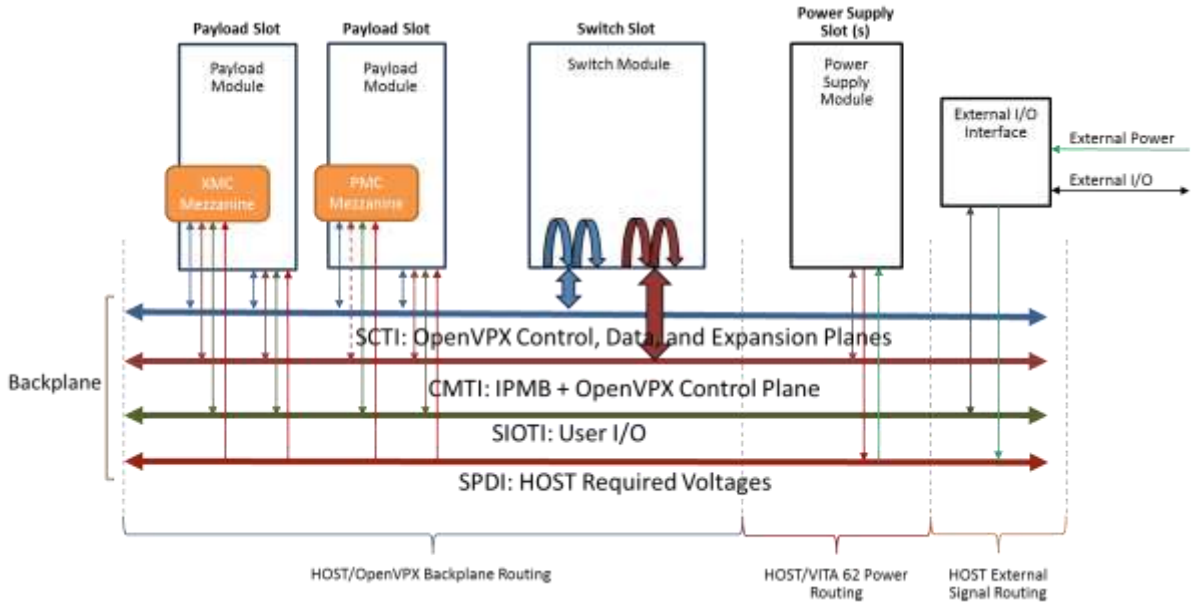


Figure 5.4-1 – HOST Tier 2 Transmission Interface Configuration

5.4.1.1 Common Transmission Interface Requirements

T2-RUL-2340: HOST Backplanes **shall** implement the requirements of ANSI/VITA 65.0, Section 7.2 through 7.4 (Common to 6U and 3U — *Backplane Profiles*).

T2-RUL-2390: Rear Transition Modules **shall** not be used to implement a Transmission Interface.

5.4.1.2 System Communications Transmission Interface Requirements

The HOST SCTI is implemented in hardware using OpenVPX switched fabric Backplane and PMC/XMC mezzanine technologies. The majority of requirements for SCTI implementations will come from the electrical and mechanical requirements of ANSI/VITA 65.0 (OpenVPX System Specification) for Backplanes. The SCTI functionality is performed by the OpenVPX Data Plane, Expansion Plane, and the non-BASE-T portion of the Control Plane high-speed serial interconnects. Functionality is extended to HOST Mezzanine Modules through PMC/XMC data bridges.

The OpenVPX Data Plane transmits low-latency, high-bandwidth system data between modules utilizing Ethernet or PCIe. The OpenVPX Data Plane is typically a centralized switched network utilizing one or more switches. The switch, or switches, are classified as being part of the SCTI. The Expansion Plane protocol is most often PCIe and is typically used for communication between adjunct Modules and not through a Switch Module, though the HOST Standard does not limit the Expansion Plane to only be used in this manner.

Mezzanine Module communications paths are also included as part of the SCTI. Mezzanine communications paths will sometimes include a bridge on the HOST Plug-In Module that translates PMC communications to the local bus of the Plug-In Module (usually PCI Express).

In cases where resources are co-located in hardware, the physical SCTI layers may be unneeded, leaving the SCTI logical communications to be performed completely within the hardware abstraction software layers.

5.4.1.2.1 Common System Communications Interface Requirements

T2-RUL-2930: The SCTI hardware components **shall** be defined as:

1. The Data Plane portion of an OpenVPX Backplane
2. The UTPs/Fat Pipes (FPs) of the Control Plane portion of an OpenVPX Backplane
3. OpenVPX conformant Plug-In network switches
4. The Expansion Plane portion of an OpenVPX Backplane

T2-OBS-0640: The SCTI is physically composed of an OpenVPX Backplane and Plug-In Switch Module(s) that perform the network packet switching.

T2-PER-0091: Although the Data Plane, Expansion Plane and Control Plane are separately labeled in a Slot Profile, Backplanes **may** connect interconnect ports labeled Data Plane, Control Plane, and Expansion Plane.

5.4.1.2.2 Mezzanine System Communications Interface Requirements

T2-RUL-2990: The SCTI **shall** include Payload Module's communications bridges to convert the SCTI protocols located on the Backplane to the appropriate PMC/XMC communications protocols for Mezzanine Modules.

T2-RUL-3000: If Payload Modules have HOST Mezzanine Module sites, SCTI communications bridges **shall** be located on the Payload Modules.

T2-PER-0180: Payload Modules that have attached mezzanines **may** be carrier boards where their only purpose is to support Mezzanine Modules.

T2-RUL-3010: The SCTI, as bridged to mezzanine slots, **shall** conform to the communications requirements of one of the following mezzanine card standards:

1. IEEE Std. 1386.1 Standard for PCI Mezzanine Cards
2. ANSI/VITA 42 Standards for Switched Mezzanine Cards

T2-RUL-3020: Requirements for SCTI mezzanine communications **shall** be applied using the following order of precedence:

1. Requirements of this Tier 2 HOST Standard (including additions or exclusions to PMC/XMC standards).
2. Mezzanine Module requirements of IEEE 1386.1 and ANSI/VITA 42.0 for PMCs and XMCs respectively.

T2-RUL-3030: The SCTI as bridged to PMC Mezzanine Modules **shall** conform to PMC 64-bit 33/66MHz PCI V2.3 communications standard.

T2-RUL-3040: The SCTI as bridged to XMC Mezzanine Modules **shall** conform to ANSI/VITA 42.3, American National Standard for XMC PCI Express Protocol Layer Standard.

T2-OBS-0650: XMC Mezzanine Modules that conform to parallel and Serial RapidIO protocols are not permitted in this standard.

5.4.1.3 System I/O Transmission Interface Requirements

The SIOTI is implemented as internal routing on the OpenVPX Backplane and connects the EIOTI with the User Defined and Thin-Pipe Ethernet pins of the HOST Plug-In Module slots. The SIOTI is intended for routing external I/O to and from modules and cannot be used for custom, inter-module communications that circumvent the chassis management, modularity, and openness of HOST.

5.4.1.3.1 Common System I/O Interface Requirements

T2-RUL-3050: The SIOTI hardware components **shall** be implemented as internal routing on the OpenVPX Backplane.

T2-PER-0185: Signals **may** be implemented over an optical fiber or coaxial cable going directly from the Platform to a Module Slot containing an ANSI/VITA 66.0 or 67.0 compliant connector.

T2-RUL-3080: All signals transmitted over a HOST Module's user defined pins **shall** be transmitted exclusively via the SIOTI.

T2-REC-0055: All signals not assigned to the SCTI, CMTI or SPDI **should** only interface with Platform I/O.

T2-OBS-0661: PMC and XMC I/O is not considered User Defined by the HOST Standard and thus can be transmitted to other PMCs and XMCs as well as External I/O Modules, but it is recommended that the Mezzanine I/O interfaces with the Platform.

T2-OBS-0660: The SIOTI connector pinouts with respect to mezzanine interfaces are referenced in SECTION 5.1.1.1.2.2.4 and SECTION 5.1.1.1.2.3.6.

5.4.1.3.2 Backplane System I/O Interface Requirements

T2-RUL-3090: The SIOTI Backplane routing **shall** provide connectivity between the SIOTI and the EIOTI.

T2-OBS-0670: The user defined signals transmitted by the SIOTI are generically defined by the Slot and Module Profiles.

5.4.1.4 External I/O Transmission Interface Requirements

This Tier 2 HOST Standard broadly defines the Backplane mechanical and electrical connector interface portions of the EIOTI giving it the flexibility to meet the mechanical and electrical constraints of a Target System. This Tier 2 HOST Standard does not define the Target System interface panel mechanical and electrical portions of the EIOTI as that is defined by the Target System requirements.

The EIOTI Interconnect Diagram is shown in FIGURE 5.4-2.

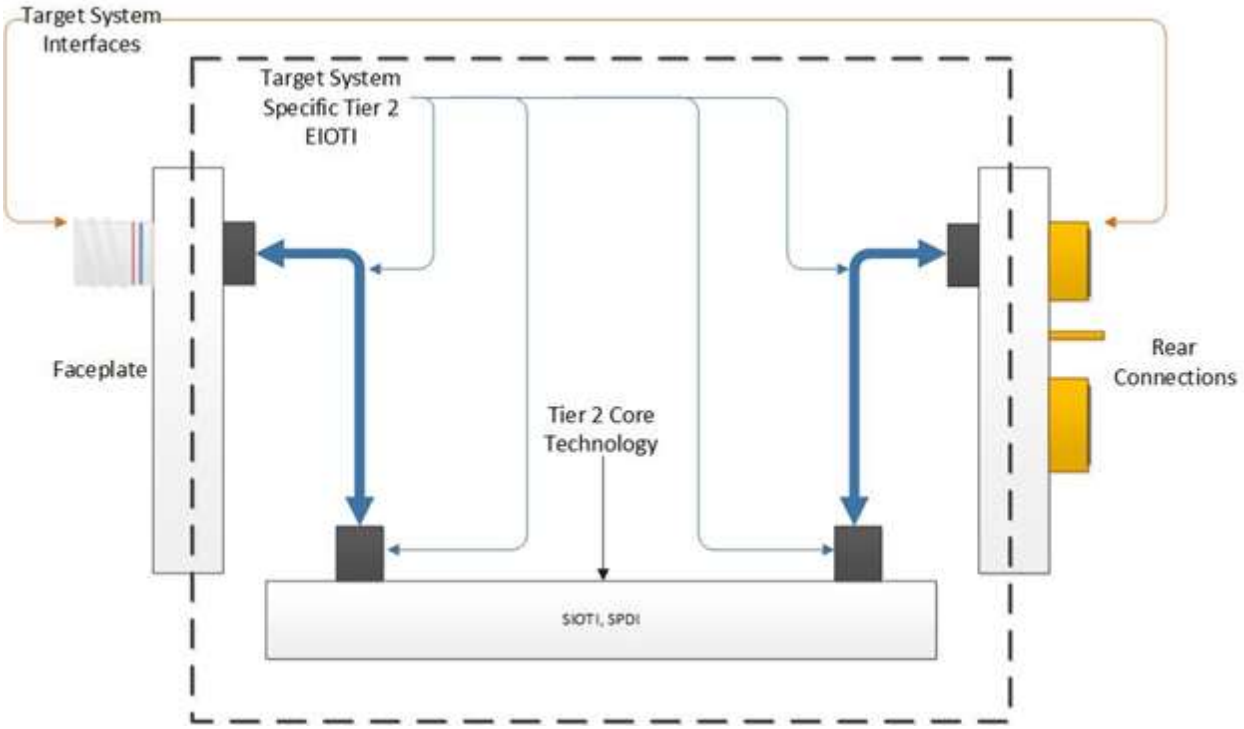


Figure 5.4-2 – HOST EIOTI Interconnect Diagram

T2-REC-0035: The EIOTI **should** be a modular unit that can be disconnected from the OpenVPX Backplane.

T2-OBS-0680: Modular EIOTI units facilitate HOST implementation migration and Target System lifecycle upgradeability and serviceability requirements.

T2-RUL-3120: The EIOTI **shall** provide connectivity between the external I/O at an Enclosure-level panel interface and the SIOTI at a Backplane interface.

T2-RUL-3130: The EIOTI **shall** provide connectivity between the Target System input power at an Enclosure-level panel interface and the SPDI at a Backplane interface.

T2-OBS-0690: The mechanical requirements for EIOTI modules are addressed in SECTION 5.4.2.

T2-RUL-3140: All external panel I/O signals **shall** pass through the EIOTI Backplane connector(s) before going to any HOST Module.

T2-PER-0195: The ANSI/VITA 66 and 67 family of blind mate connectors **may** be considered an EIOTI Backplane connector.

T2-OBS-0700: External front or rear panel chassis I/O signals include video and power.

T2-RUL-3150: All SIOTI Interface signals **shall** pass through the EIOTI Backplane connector(s) before going to any external front or rear panel chassis I/O connectors.

T2-OBS-0705: When connecting the front/rear panel connectors directly to the Backplane, those connectors are considered the EIOTI Backplane connectors.

T2-RUL-3170: All EIOTI Backplane connectors **shall** be commercially available connectors that can be procured by any vendor without prior authorization from any source (e.g. a commercial part governed by a source control drawing).

T2-RUL-3180: The EIOTI **shall** provide a path for connecting chassis ground to the SPDI at the HOST Backplane in support of ANSI/VITA 65.0, Section 3.2.3, Safety Ground.

5.4.1.5 Chassis Management Transmission Interface Requirements

The CMTI is implemented in hardware using OpenVPX Backplane technology. The majority of requirements for CMTI implementations will come from the electrical and mechanical requirements of ANSI/VITA 65.0 (OpenVPX System Specification) for Backplanes. CMTI functionality is performed by portions of the OpenVPX Control Plane, the OpenVPX Utility Plane and the OpenVPX Management Plane implementing ANSI/VITA 46.11. The OpenVPX Control Plane may be used for transmission of messages and large data transfers such as *Operational Flight Program* (OFP) loading. The OpenVPX Utility Plane includes power distribution functions and common control/status signals. The CMTI only includes the control/status functions of the OpenVPX Utility Plane. The OpenVPX Management Plane is implemented using the IPMB, where the Backplane contains the physical bus portion of the IPMB and Plug-In Modules contain an IPMC.

5.4.1.5.1 Common Chassis Management Transmission Interface Requirements

T2-RUL-3190: The CMTI hardware components **shall** be implemented utilizing:

1. The Backplane-routed control and status portions of the OpenVPX Utility Plane
2. The IPMB OpenVPX Management Plane
3. The UTP Control Plane Ethernet

T2-RUL-3270: HOST Backplanes **shall** implement a pull-up resistor from each CMTI IPMB signal to the 3.3V Auxiliary voltage rail.

T2-OBS-0750: The pull-up resistor requirement supersedes ANSI/VITA 46.0 Rule 7-1, requiring spare resistors for both single-ended and differential termination schemes, and its value is described in ANSI/VITA 46.11 Section 9.2.3-1, System IPMB Pull-Up Resistors.

T2-RUL-3280: HOST Modules **shall** have zero pull-up resistors on the CMTI IPMB signals.

T2-OBS-0760: The rule against HOST Modules having pull-up resistors on the IPMB is a clarification of ANSI/VITA 46.11, Rule 9.2.3-2.

T2-RUL-3290: HOST Modules containing resources to drive the Utility Plane REF_CLK+/- signals **shall** provide a mechanism to permit Application Software or system management to reassign the identity of the SYS_CON module, regardless of the logic level of the Backplane SYS_CON* contact, in order to control these signal drivers once the Backplane power rails are all at minimum operating voltages as defined in ANSI/VITA 46.0, Section 4.8.12.4.

T2-OBS-0765: The SYS_CON module identity reassignment is a Recommendation 3.4.1-1 in ANSI/VITA 65.0.

T2-RUL-3291: The NVMRO portion of the CMTI **shall** conform to the low current open-drain signal specifications of ANSI/VITA 65.0, Section 3.3.1.

T2-RUL-3300: The SYSRESET* portion of the CMTI **shall** conform to the high current open-drain signal specifications of ANSI/VITA 65.0, Section 3.3.3 (High Current Open-Drain).

T2-RUL-3310: HOST Plug-In Modules receiving SYSRESET* as an input **shall** be able to register a valid low for any pulse length of 10ms or longer.

T2-RUL-3320: Payload Modules **shall** make SYSRESET* available to any HOST Mezzanine Module connector that has SM1 and SM0 available per ANSI/VITA 65.0, Recommendation 3.4.2.1-1.

T2-RUL-3321: The Backplane **shall** provide a method for optionally pulling the SYS_CON* signal low for all VPX Slots.

T2-RUL-3322: GAP* and GA[4:0] **shall** be wired to indicate physical slot numbers, with the numbers going from 1 thru N, where N is the number of slots.

T2-RUL-3330: HOST Plug-In Modules **shall** receive a unique Site Number that is based upon the Module's ANSI/VITA 65.0, Section 3.4.6, Geographic Address.

T2-OBS-0770: ANSI/VITA 65.0, Section 3.4.6, Geographic Address Field, specifies how geographical addressing is accomplished for OpenVPX modules.

T2-OBS-0775: It is recommended in ANSI/VITA 46.0 that *Joint Test Action Group* (JTAG) pins not be bussed on Backplanes.

T2-OBS-0790: ANSI/VITA 65.0, Section 3.4.7, JTAG Port, specifies that each P0/J0 connector must support the JTAG signal assignment established in ANSI/VITA 46.0. The JTAG port is designated for single-card use outside of the Target System only. For example, it can be used for single-card manufacturing, programming, or debug purposes.

T2-RUL-3370: The Control Plane as defined in SECTION 5.1.1.1.2 and SECTION 5.1.1.1.3 **shall** be included as part of the CMTI.

T2-RUL-3371: If a Level A Conformant Payload Module has an XMC Mezzanine site, the Level A Conformant Payload Module **shall** route the ANSI/VITA 42.0 defined I2C connections from the XMC Mezzanine Site to the IPMC of the Payload Module.

T2-OBS-0792: XMC Mezzanine Modules conform to the requirements for supporting the CMTI through the IPMC located on the parent Payload Modules. An example is illustrated in FIGURE 5.4-3.

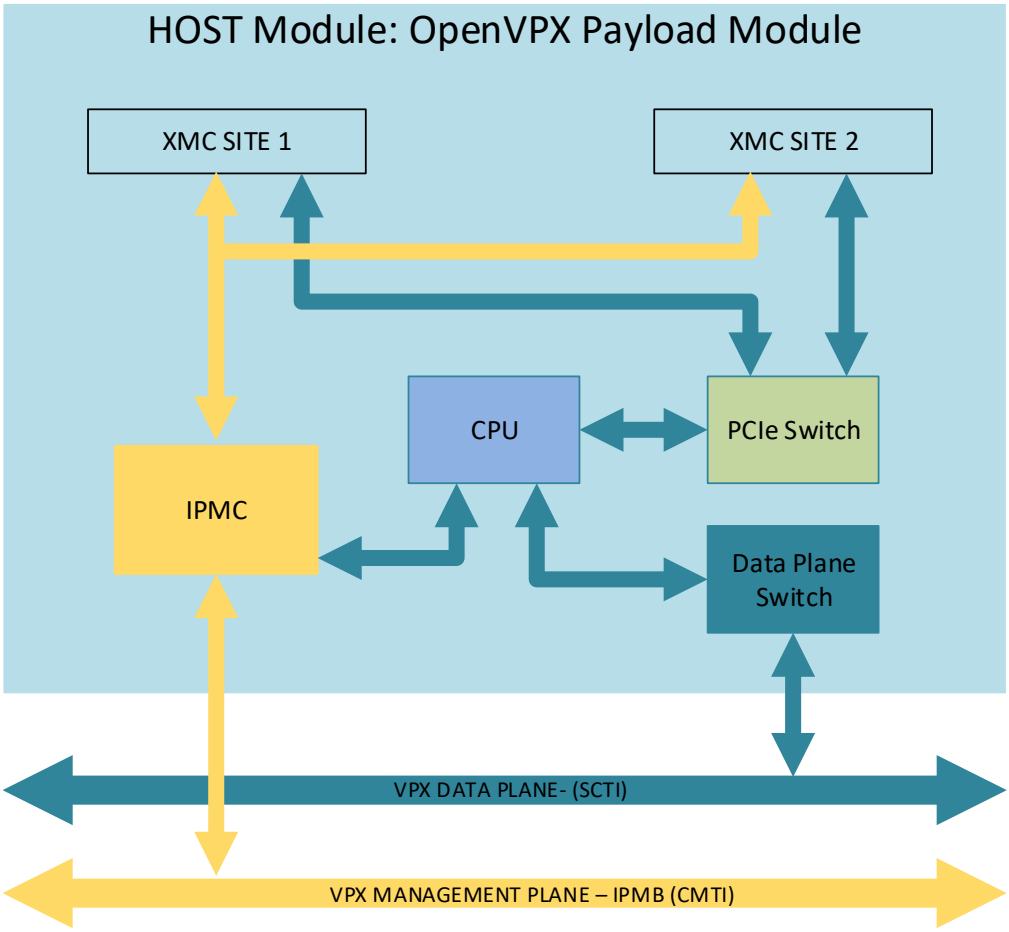


Figure 5.4-3 – Example HOST Payload Module XMC Mezzanine CMTI Configuration

T2-OBS-0793: PMC Mezzanine Modules conform to the requirements for supporting the CMTI through the parent Payload Module utilizing software components. An example is illustrated in FIGURE 5.4-4.

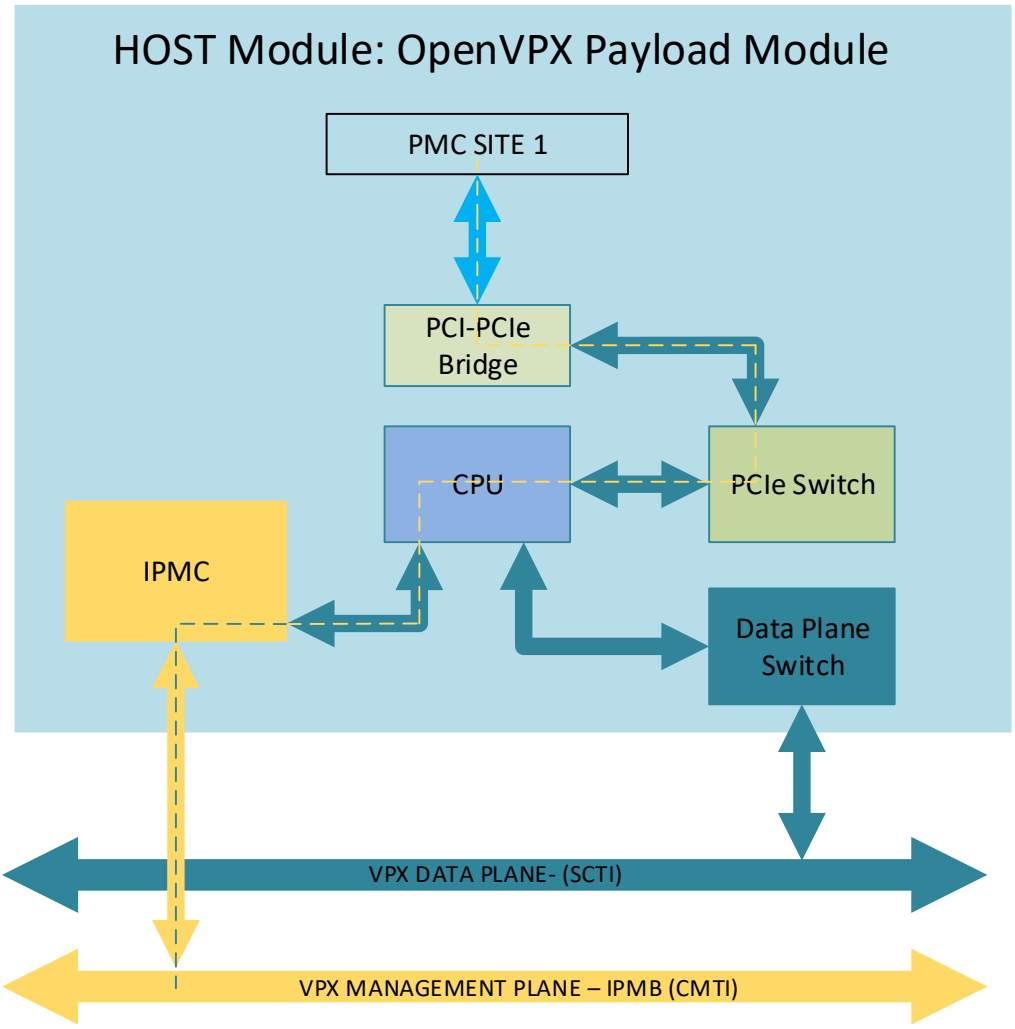


Figure 5.4-4 – Example HOST Payload Module PMC Mezzanine CMTI Configuration

5.4.1.5.2 6U Chassis Management Interface Requirements

T2-RUL-3220: The 6U hardware components implementing the IPMB Management Plane **shall** conform to the electrical requirements of ANSI/VITA 46.11 as applied to 6U OpenVPX implementations except where specified herein.

T2-RUL-3250: The 6U CMTI electrical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 6U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-RUL-3260: The 6U CMTI mechanical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 6U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-OBS-0710: HOST power distribution is accomplished with the SPDI.

T2-OBS-0730: ANSI/VITA 65.0, Section 3.3, Electrical Standards for Drivers and Receivers, specifies the electrical parameters for the OpenVPX Utility Plane.

T2-OBS-0740: ANSI/VITA 65.0, Section 3.4, System Control Signals, defines the OpenVPX Utility Plane signals and their functionality.

5.4.1.5.3 3U Chassis Management Interface Requirements

T2-RUL-3261: The 3U hardware components implementing the IPMB Management Plane **shall** conform to the electrical requirements of ANSI/VITA 46.11 as applied to 3U OpenVPX implementations except where specified herein.

T2-RUL-3262: The 3U CMTI electrical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 3U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-RUL-3263: The 3U CMTI mechanical parameters **shall** conform to the ANSI/VITA 65.0 OpenVPX Utility Plane requirements for 3U OpenVPX implementations excluding ANSI/VITA 65.0, Section 3.2, Power Distribution.

T2-OBS-0741: HOST power distribution is accomplished with the SPDI.

T2-OBS-0742: ANSI/VITA 65.0, Section 3.3, Electrical Standards for Drivers and Receivers, specifies the electrical parameters for the OpenVPX Utility Plane.

T2-OBS-0743: ANSI/VITA 65.0, Section 3.4, System Control Signals, defines the OpenVPX Utility Plane signals and their functionality.

T2-OBS-0744: 3U Power Supply Modules only have GA[1:0] due to pin count. If it is desired that the PSM be higher than slot 4, offset logic will need to be implemented. For example, a specific Backplane power supply start at logical slot 6, for 3U PSMs GA1 GND and GA0 Open would mean logical slot 7.

5.4.1.6 System Power Distribution Interface Requirements

The HOST SPDI primary function is distributing power to Plug-In Modules. The SPDI distributes defined voltages to each VPX slot on the HOST Backplane via the OpenVPX Utility Plane. The ANSI/VITA 65.0, signals VS1, VS2, VS3, 3.3V_AUX, and +/-12V_AUX of the OpenVPX Utility Plane make up the SPDI. The SPDI is also responsible for transporting prime power to the *Power Supply Resource* (PSR) and intermediate power between PSR stages and/or to Energy Storage Modules described in SECTION 5.1.1.2.

5.4.1.6.1 Common System Power Distribution Interface Requirements

T2-RUL-3420: The SPDI **shall** conform to the Backplane requirements of ANSI/VITA 65.0, Section 3.2 except where specified herein.

T2-RUL-3430: For HOST VPX Slots the SPDI **shall** exclusively support the Power Distribution portion of the OpenVPX Utility Plane.

T2-RUL-2360: HOST Backplanes **shall** size Vs1 to be able to distribute at least 14 A per slot. Refer to connector current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-RUL-2365: HOST Backplanes **shall** size Vs2 to be able to distribute at least 14A per slot. Refer to connector current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-OBS-0073: The power distribution requirements for VS1, VS2 and VS3 are requirements on the ability to provide power to each individual slot, but is not meant to require the backplane to handle the case where every slot is pulling the required loads simultaneously.

T2-RUL-2375: HOST Backplanes **shall** have a 4.7K pull-up on the PSM slot's FAIL* signal, as is recommended in Observation 4.6.3.7-1 of ANSI/VITA 62.0.

T2-RUL-3460: If a Payload Module supports a PMC site, a Payload Module **shall** route the SPDI to the appropriate PMC connectors per IEEE 1386.1.

T2-RUL-3465: If a Payload Module supports a XMC site, a Payload Module **shall** route the SPDI to the appropriate XMC connectors per ANSI/VITA 42.0.

T2-OBS-0820: Due to the site profile provided for PMCs, a Payload Module implementing that site profile will need to route the SPDI to both the XMC and PMC connectors.

T2-RUL-3470: The SPDI **shall** conform to the requirements for Single-Stage or Two-Stage power subsystems as specified by ANSI/VITA 62.0.

T2-OBS-0830: If a subsystem requires any Energy Storage Modules then the SPDI also must support the Energy Storage Module.

T2-RUL-3480: The SPDI **shall** provide a Backplane interface connector for transmitting Platform power from the EIOTI to the SPDI.

T2-RUL-3490: The SPDI **shall** receive a chassis ground signal from the EIOTI.

5.4.1.6.2 6U System Power Distribution Interface Requirements

T2-RUL-3491: The SPDI for 6U systems **shall** conform to the 12V High Voltage Power Input requirements of ANSI/VITA 46.0, Section 4.8.1.1.3.

T2-RUL-3400: The SPDI for 6U component interfaces **shall** conform to the 6U Backplane electrical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-RUL-3410: The SPDI for 6U component interfaces **shall** conform to the 6U Backplane mechanical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-OBS-0810: Some sections of ANSI/VITA 62.0 and 65.0 contain requirements for air-cooled modules only. These requirements are not applicable to this Tier 2 technology.

T2-RUL-2370: HOST Backplanes **shall** size Vs3 to be able to distribute at least 22 A per 6U slot. Refer to current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-OBS-0811: The power rail sizes are the recommended minimums from ANSI/VITA 65.0, Section 11.2.1.2.1.

5.4.1.6.3 3U System Power Distribution Interface Requirements

T2-RUL-2374: The SPDI for 3U system **shall** conform to the High Voltage Power Input requirements of ANSI/VITA 46.0, Section 4.8.1.1.4.

T2-RUL-2371: The SPDI for 3U component interfaces **shall** conform to the 3U Backplane electrical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-RUL-2372: The SPDI for 3U component interfaces **shall** conform to the 3U Backplane mechanical requirements of ANSI/VITA 62.0 standard for Modular Power Supplies except where specified herein.

T2-OBS-0812: Some sections of ANSI/VITA 62.0 and 65.0 contain requirements for air-cooled modules only. These requirements are not applicable to this Tier 2 technology.

T2-RUL-2373: HOST Backplanes **shall** size Vs3 to be able to distribute at least 15 A per 3U slot. Refer to current load limits in ANSI/VITA 46.0, Section 4.8.1.

T2-OBS-0813: The power rail sizes are the recommended minimums from ANSI/VITA 65.0, Section 15.2.1.2.1.

5.4.2 HOST Components

A notional layout for a HOST implementation is presented in FIGURE 5.4-5. This figure shows a hypothetical design to provide clarification for HOST Component descriptions. Layouts for specific Enclosure designs will vary.

As seen in the figure, the system for this Tier 2 technology comprises components from four categories, defined in the following sections:

- **HOST Enclosure –** The Enclosure design is variable and is designed to suit the requirements of the Target System. In the following notional views, it is approximated by a standard 1 ATR Enclosure, defined in ARINC 404A.
- **HOST Module –**Payload Module, Switch Module, External I/O Module, PMC/XMC Mezzanine Module, or Power Supply Module.
- **HOST Backplane –** A physical circuit card assembly that accepts HOST Plug-In Modules and provides access to HOST Transmission Interfaces. The transmission components may also consist of discrete wires or cable assemblies serving as the connection between HOST Modules and *HOST External Interfaces*.
- **HOST External Interfaces –** External interfaces transfer signals and power between the HOST Transmission Components and the external system.

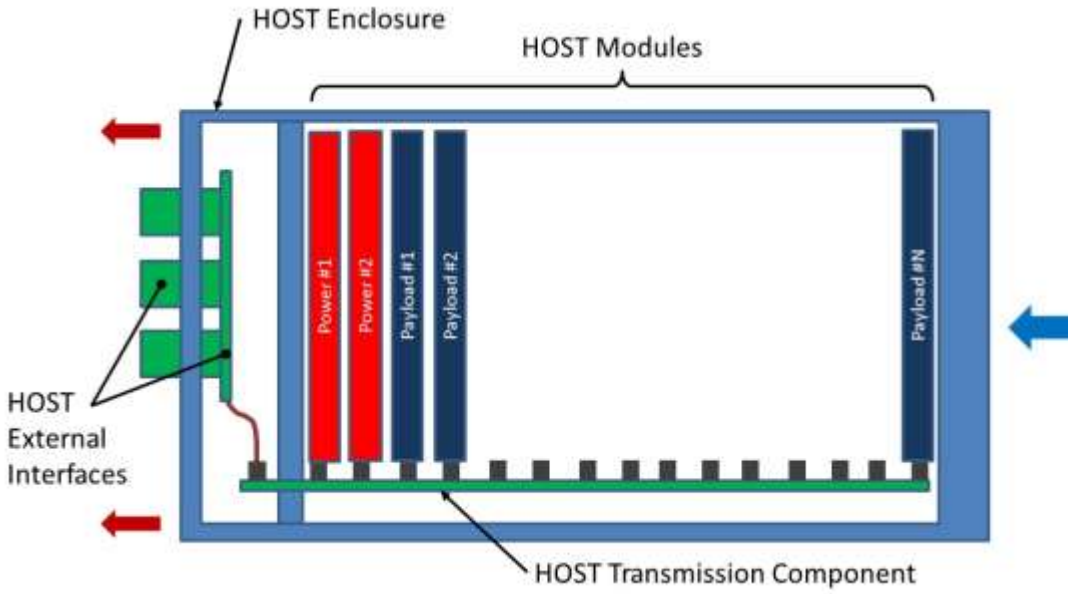


Figure 5.4-5 – Notional Side View of a Generic ATR Mission Computer

5.4.2.1 HOST Components Common Environmental Requirements

Hardware environmental requirements are ultimately determined by the natural and induced environmental conditions at the deployed location(s) of the system. These requirements can span from benign conditions such as office/laboratory spaces to extreme military vehicles. Environmental requirements are validated by the test methods listed in ANSI/VITA 47 dot standards, MIL-STD-810, or DO-160. Specific environmental requirements for HOST Enclosures, External Interfaces, and Transmission Components are defined at the Target Platform Level. Below is a list of these environmental conditions; not all are applicable for each platform or applicable to all hardware components.

High and Low Temperatures during storage
High and Low Temperatures during operations
Low Pressure (Altitudes, during air transport and operations)
Handling Shock
Transportation Vibration (truck and air transport)
Explosive Atmosphere
Condensation
Condensation Drip
Acceleration
Operational Vibration
High Temperatures, Solar Induced
Salt (corrosion)
Thermal Shock
Sand/Dust Impingement
Fungus
Humidity

T2-OBS-0814: Dependent on the platform, the environmental requirements can be found in specific equipment performance specifications or system specifications. Most military requirements use MIL-STD-810 test methods.

T2-REC-3510: All environmental claims **should** be subject to a physical test.

T2-OBS-0815: Physical tests may be replaced by computer simulations if the simulation data has previously been verified by physical test, at the discretion of the acquiring authority.

T2-OBS-0816: Environmental claims may be proved by analysis or similarity with approval of the acquiring authority.

T2-RUL-3515: Environmental test results **shall** specify, at a minimum, the test procedure/method, test equipment and test data.

T2-OBS-0817: Complete listings of test methods, classes, and test levels allows integrators and system designers to quickly determine if components that conform to a given environmental specification are rated to the environmental conditions for a particular application/platform.

5.4.2.2 HOST Enclosure

5.4.2.2.1 Form Factor

T2-OBS-0840: External form factor requirements will be dictated by the requirements of the Target System.

T2-RUL-3520: The VPX Module region of the HOST Enclosure **shall** house VPX Modules as defined by SECTION 5.1.1.1.

T2-RUL-3540: The Power Supply Module region of the HOST Enclosure **shall** house power supply modules as defined in SECTION 5.1.1.2.

5.4.2.2.2 Card Cage Environment and Form Factor

T2-RUL-3550: The HOST Enclosure **shall** have rail geometry in accordance with IEEE 1101.2-1992 (R2008). Note: IEEE-1101.2-1992 (R2008) uses the term “Card Guide Slots” instead of “Rails”.

T2-RUL-3560: The card cage rail **shall** have a pitch of 1-inch for all electronic module slots.

T2-OBS-0850: The rail geometry for 6U is further specified in FIGURE 5.4-6 and the rail geometry for 3U is further specified in FIGURE 5.4-7.

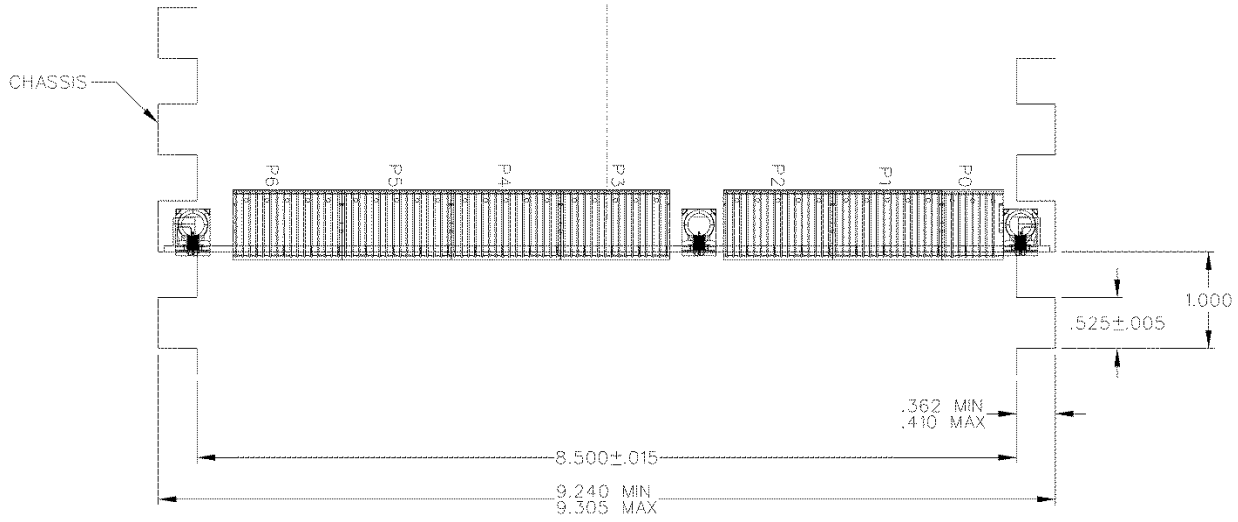


Figure 5.4-6 – 6U Rail Geometry

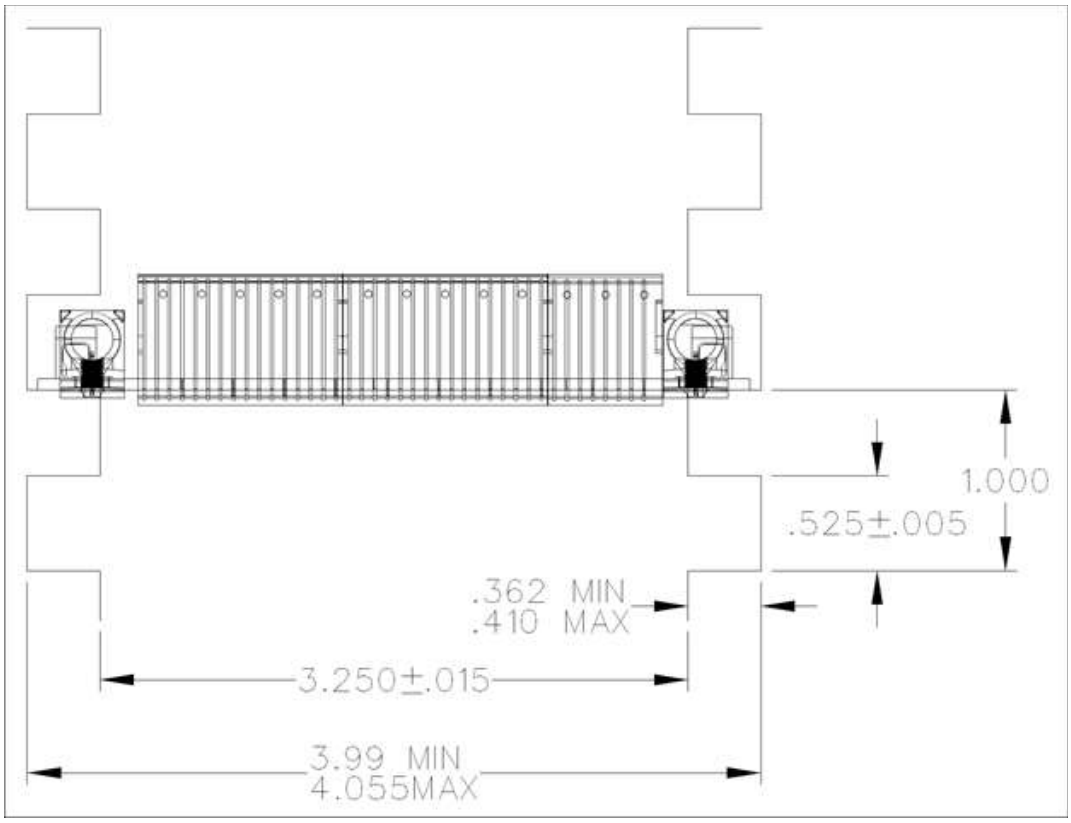


Figure 5.4-7 – 3U Rail Geometry

T2-RUL-3570: The card cage **shall** utilize wedgelocks as defined in ANSI/VITA 46.0, Appendix A.

T2-RUL-3580: The HOST Enclosure card cage **shall** provide conduction cooling to the electronic modules.

5.4.2.3 HOST Module

The standards of this section define the module requirements for the Tier 2 Standard.

5.4.2.3.1 Form Factor

The form factor for standard HOST VPX Modules is defined in ANSI/VITA 65.0, Section 4. ANSI/VITA 65.0 passes the majority of these requirements through from ANSI/VITA 46.0 and ANSI/VITA 48 dot standards, which refer to standard form factors defined in IEEE 1101.1 and IEEE 1101.2. HOST recommends following ANSI/VITA 48.2, IEEE 1101.1, and IEEE 1101.2 for guidance regarding form factor of HOST 6U and 3U Modules.

T2-RUL-3610: VPX Modules **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 65.0 for conduction cooled modules
3. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

T2-RUL-3630: PMC Mezzanine Modules **shall** adhere to form factor constraints provided in IEEE 1386.

T2-RUL-3631: XMC Mezzanine Modules **shall** adhere to form factor constraints provided in ANSI/VITA 42.0.

T2-RUL-3640: HOST Mezzanine Modules **shall** pass qualification testing while installed on the Payload Module including all hardware and accessories.

T2-OBS-0870: HOST Mezzanine Modules may undergo preliminary testing, but it is a higher priority to characterize the effect of Mezzanine Modules on other resources.

5.4.2.3.2 Interfaces

T2-RUL-3670: HOST Plug-In Modules **shall** use alignment-keying sockets defined in ANSI/VITA 46.0, Table 4-2.

T2-RUL-3680: HOST Plug-In Modules **shall** use alignment keys as defined in ANSI/VITA 46.0, Section 4.4.3 Plug-In Module Key.

T2-PER-0011: HOST Plug-In Modules **may** use the Ruggedized Machined 6061 Aluminum RT2-R compatible keying guide sockets.

T2-OBS-0880: The actual keying positions of the Plug-In Modules will depend on the orientation of the keying pins of the HOST Backplane slot the baseboard is interfacing with.

T2-REC-0045: With higher shock and vibration environments, VPX Modules **should** use the 3700, or equivalent.

T2-REC-0046: Alignment pin keying information for Plug-In Modules **should** be documented.

T2-RUL-3700: VPX Modules **shall** use the connectors defined for the Slot Profile of the VPX Module as specified in ANSI/VITA 65.0 and ANSI/VITA 65.1.

T2-PER-0207: VPX Modules **may** use RT 2-R, RT 3, or equivalent connectors when the connector is specified in ANSI/VITA 65 to use VITA 46.0 connectors.

T2-OBS-0881: Certain Slot Profiles specify the use of blind-mate optical and coax connectors in place of the differential connectors.

T2-RUL-3720: HOST Plug-In Modules **shall** prohibit features that prevent installation in a HOST Enclosure.

T2-RUL-3730: No additional components **shall** be required to install a Plug-In Module in a HOST Enclosure other than those typically used for ANSI/VITA compliant OpenVPX modules.

5.4.2.3.2.1 6U Interfaces

T2-RUL-3690: 6U Power Supply Modules **shall** follow the rules defined in ANSI/VITA 62.0, Section 4.3.2 6U Slot Keying and in Section 6.3 Alignment and Keying.

5.4.2.3.2.2 3U Interfaces

T2-RUL-3701: 3U Power Supply Modules **shall** follow the rules defined in ANSI/VITA 62.0, Section 4.3.1 3U Slot Keying and in Section 5.3 Alignment and Keying.

5.4.2.3.3 HOST Module Environmental Requirements

T2-RUL-3743: A HOST Module **shall** conform to an approved environmental specification, provided alongside a Tier 3 Specification.

T2-REC-0048: HOST Modules **should** conform to one, or more, of the environmental classes called out in ANSI/VITA 47.x.

T2-OBS-0896: VITA 47.x meets the requirements for an environmental specification and also is closely aligned to the environmental requirements of ruggedized systems.

T2-REC-0049: The differences between the environmental specification met by a HOST Module and the closest ANSI/VITA 47.x class **should** be documented.

T2-OBS-0891: TABLE 5-6 shows how ANSI/VITA 47.x links to MIL-STD-810 test methods and procedures.

Table 5-6 Module Environmental Requirements

Environment	ANSI/VITA 47.x Section	MIL-STD-810 Method, Procedure
Operating Temperature	4.1	Method 501, 502 Procedure II
Non-Operating Temperature	4.2	Method 501, 502 Procedure I
Temperature Cycling*	4.3	MIL-STD-202, Method 107
Vibration	4.4	Method 514, Procedure I
Shock, Operating and Bench Handling	4.5	Method 516, Procedure I, VI
Humidity	4.6	Method 507
Altitude, Operating	4.7	Method 500, Procedures II
Rapid Decompression	4.8	Method 500, Procedures III
Attitude*	4.9	N/A
Fungus Resistance	4.10	Method 508
Electrostatic Discharge Resistance (With Optional Covers)*	4.11	EN61000-4-2
Corrosion Resistance*	4.12	ASTM G85

*Not Covered by MIL-STD-810 Methods

T2-PER-0210: A HOST Module validated to a particular ANSI/VITA 47.x environmental class **may** be automatically qualified to a lower ANSI/VITA 47.x environmental class.

T2-OBS-0892: Selection of the class listed in ANSI/VITA 47.x depends on the ruggedness level desired for the environmental conditions anticipated while in use.

T2-OBS-0893: Conditions a module will experience within a particular enclosure could differ from the enclosure level requirements. Consult the enclosure designer for vibration and temperature conditions within the enclosure.

T2-OBS-0894: Additional requirements may be required by platform program offices or integrators for very extreme environmental conditions.

T2-OBS-0895: ANSI/VITA 47.2 and ANSI/VITA 47.3 introduce additional workmanship requirements on top of the environmental requirements. ANSI/VITA 47.2 introduces requirements for conforming to at least IPC J-STD-001 Class 2 and ANSI/VITA 47.3 introduces requirements for conforming to IPC J-STD-001 Class 3. The majority of HOST Modules are expected to be categorized as Class 3 Electronic Products.

T2-RUL-3780: Conformal coating for HOST Modules **shall** be applied per IPC J-STD-001F.

T2-RUL-3790: Materials used for conformal coating **shall** conform to IPC-CC-830.

5.4.2.4 HOST Transmission Components

HOST Transmission Components facilitate physical connectivity of power and communications signals between HOST Modules. The standard transmission component for OpenVPX is a Backplane that interfaces with standard Plug-In Modules. This standard defines the required form factor, interfaces, environmental requirements, and documentation requirements for the HOST OpenVPX Backplane.

5.4.2.4.1 Form Factor

The form factor for standard HOST OpenVPX Backplane is defined in ANSI/VITA 65.0, Section 4. ANSI/VITA 65.0 essentially passes these requirements through from ANSI/VITA 46, which refer to standard form factors defined in IEEE 1101.1 and IEEE 1101.2. FIGURE 5.4-8 shows the required 6U slot form factor derived from these standards and FIGURE 5.4-9 shows the required 3U slot form factor.

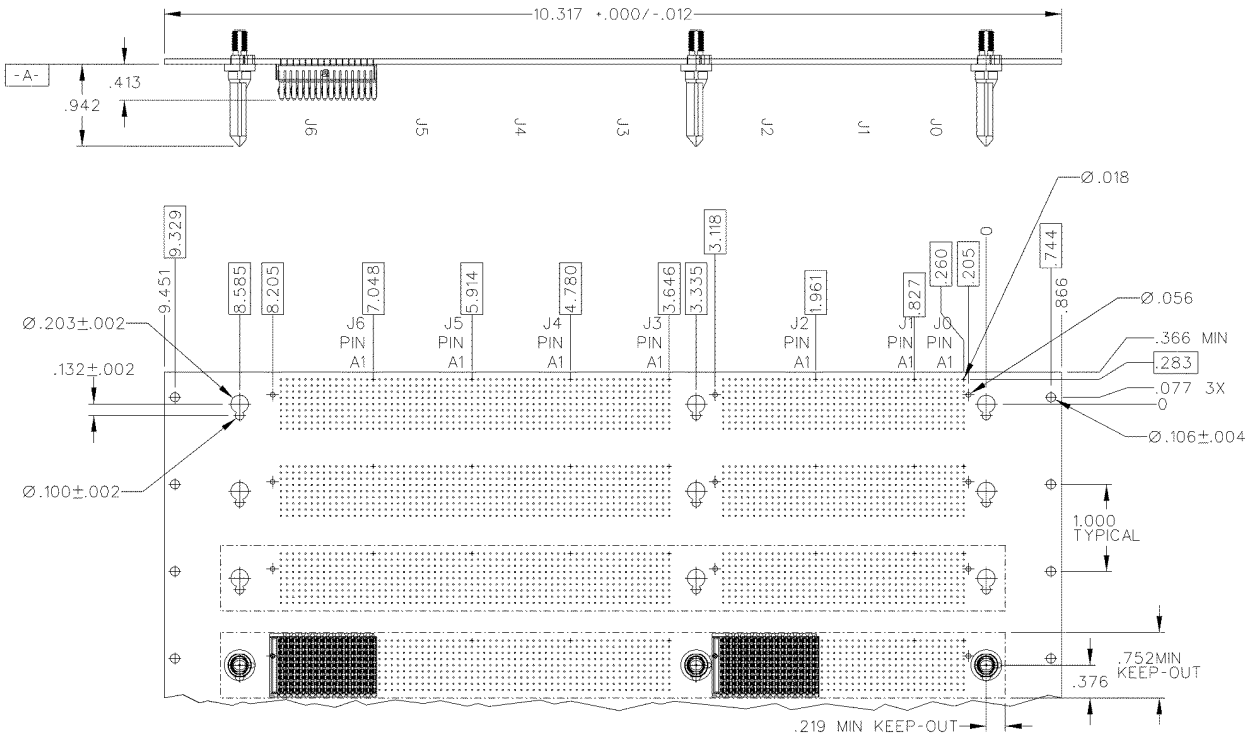


Figure 5.4-8 – 6U OpenVPX Backplane Form Factor

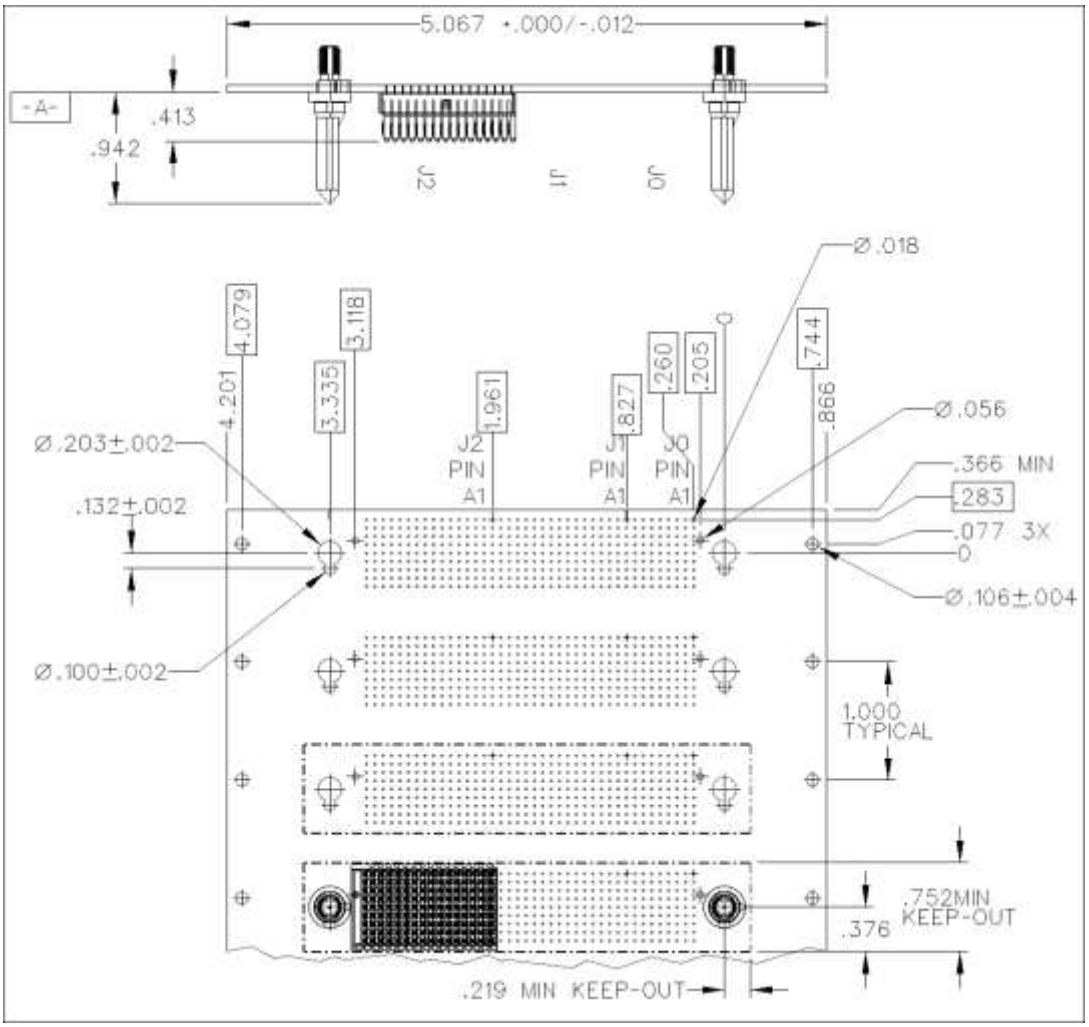


Figure 5.4-9 – 3U OpenVPX Backplane Form Factor

T2-OBS-0900: FIGURE 5.4-8 and FIGURE 5.4-9 are derived from the requirements in ANSI/VITA 65.0. For clarification, refer to ANSI/VITA 65.0 and its related documents.

T2-RUL-3800: HOST Backplanes **shall** conform to the form factor requirements of the following standards in the given order of precedence:

1. Requirements of this Tier 2 HOST Standard
2. Requirements of ANSI/VITA 65.0 for conduction cooled modules
3. Requirements of ANSI/VITA 48.2 standard for conduction cooled modules
4. Requirements of ANSI/VITA 46.0 for conduction cooled modules

5.4.2.4.2 Interfaces

T2-RUL-3810: HOST Backplanes **shall** conform to the interface requirements defined in ANSI/VITA 65.0.

T2-RUL-2480: HOST Backplanes **shall** have a 1-inch slot pitch.

T2-OBS-0901: HOST Backplanes are designed for interfacing to HOST Modules with 1-inch pitch; however, HOST Modules with 0.8-inch and 0.85-inch pitches are also allowed.

T2-RUL-3820: HOST Backplane VPX, Power Supply, and Energy Storage Slots **shall** use alignment and keying pins called out in ANSI/VITA 46.0, Observation 7-22.

T2-RUL-3890: Power supply module slots **shall** use connectors defined in ANSI/VITA 62.0, Table F-1.

T2-RUL-3880: VPX slots **shall** use the connectors defined for its specified Slot Profile as specified in ANSI/VITA 65.0 and ANSI/VITA 65.1.

T2-PER-3883: VPX slots **may** use RT 2-R, RT 3, or equivalent connectors when the connector is specified in ANSI/VITA 65 to use VITA 46.0 connectors.

T2-OBS-0913: Certain Slot Profiles specify the use of blind-mate optical and coax connectors in place of the differential connectors.

T2-REC-0047: Alignment pin keying information for HOST Backplanes **should** be documented.

T2-RUL-3910: Transmission components **shall** prohibit features that prevent installation of a HOST Module.

T2-RUL-3920: No additional non-COTS components **shall** be required to install a HOST Module.

5.4.2.4.3 6U Interface Requirements

T2-RUL-3830: HOST Backplane 6U Power Supply Module Slots **shall** be keyed in accordance to ANSI/VITA 62.0, Section 4.3.2 6U Slot Keying.

T2-RUL-3840: Key position 1 for HOST Backplane 6U VPX slots **shall** be set to 315 degrees.

T2-OBS-0078: The numbering for the key positions is called out in ANSI/VITA 46.0, Rule 4-12.

5.4.2.4.4 3U Interface Requirements

T2-RUL-3881: HOST Backplane 3U Power Supply Module Slots **shall** be keyed in accordance to ANSI/VITA 62.0, Section 4.3.1 3U Slot Keying.

T2-OBS-0911: The numbering for the key positions is called out in ANSI/VITA 46.0, Rule 4-12.

5.4.2.4.5 HOST Transmission Components Environmental Requirements

T2-RUL-3940: Conformal coating for HOST Backplanes **shall** be applied per IPC J-STD-001F.

T2-RUL-3950: Materials used for conformal coating **shall** conform to IPC-CC-830.

6 Glossary

Term	Definition
Analysis	Analysis is an element of verification that uses generally accepted technical methods, including mathematical models or simulations, algorithms, charts, graphs, circuit diagrams, data, or other scientific principles and procedures to determine conformance with specified requirements. “Generally accepted”, in this context, means in accordance with common design engineering practices.
Acquisition Authority	The Government Program office responsible for the Target System.
Active Chassis Manager	A Chassis Manager who is actively using the IPMB with address 20h and is responsible for providing the System Manager Interface.
Backplane Profile	A physical definition of a backplane implementation that includes details such as the number and type of slots that are implemented and the topologies used to interconnect them. Ultimately a Backplane Profile is a description of channels and buses that interconnect slots and other physical entities in a backplane.
Backup Chassis Manager	A Chassis Manager who is passively monitoring the IPMB in order to determine when it should become Active Chassis Manager.
Chassis Management Transmission Interface	The CMTI provides connectivity between Chassis Management entities (Chassis Managers, and IPMCs). The CMTI provides chassis management and utility capabilities such as health monitoring, status reporting, maintenance, system reset, system power-up/power-down management, and system recovery. The CMTI can share a physical transmission medium with other transmission interfaces, but it remains logically distinct based upon the type of data that it carries.
Chassis Manager	The Chassis Manager is a software or firmware entity that manages IPMCs within the Chassis Domain. The Manager communicates with IPMC via the CMTI. This standard allows the usage of two kinds of Chassis Manager: an active Chassis Manager and a backup Chassis Manager.
Commercial-Off-the-Shelf	A commercial item sold in substantial quantities in the commercial marketplace and offered to the government without modification under a contract or subcontract in the same form in which it was sold in the marketplace.
Conformance Verification and Applicability Matrix	CVAM is an appendix in HOVM that contains entries for all HOST Tier 2 requirements. It identifies the requirement ID, applicability of the requirement to the specific types of components identified in the Tier 2 Standard, recommended verification method for the requirement, and other additional information as necessary, for each Tier 2 rule.

Term	Definition
Demonstration	Demonstration is an element of verification that involves the qualitative exhibition of functional performance. While test equipment might be required as part of the Demonstration setup, measurements are typically not required. Demonstration might also be used when requirements or specifications are given in statistical terms (e.g., average power consumption, mean time to repair, etc.).
External I/O Transmission Interface	The EIOTI provides a method for connecting Platform I/O and power signals to the SIOTI and SPDI where they can then be accessed by I/O processing and PSRs. The EIOTI will typically take the form of front and/or rear panel chassis I/O connection systems that utilize any combination of cabling, rigid printed wiring board (PWB), or flex PWB.
Functional Resources	FRs perform the main functions of the system. Functions may include, but are not limited to processing of the I/O, image processing, data processing, general purpose processing, data storage, etc. These resources differ from PSRs and Chassis Management in that those architectural elements exist to support the FRs.
Field Replaceable Unit	An electronic hardware component that can be removed and replaced without sending the product to a repair facility. Throughout this Tier 2 HOST Standard, “FRU” should be interpreted as “HOST Module.”
HOST Backplane	A physical circuit card assembly that accepts HOST Plug-In Modules and provides access to the Transmission Interfaces.
HOST Conformant	An article is HOST Conformant if and only if the Tier 3 Specification and/or Module has completed the HOST Conformance Verification Process and been Gatekeeper Approved. For a module, this entails demonstration of strict adherence to a HOST Conformant Tier 3 Specification’s requirements. For a Tier 3 Specification, this requires proper documentation of the requirements levied on a module in accordance with the tenets of the Tier 3 Specification Guide.
HOST Conformant Module	A component adhering to the definition of a HOST Module that has been verified and registered.
HOST Conformant Tier 3 Specification	A document adhering to the definition of a Tier 3 Specification that has been verified and registered.
HOST Chassis	A HOST Chassis is the aggregate collection of HOST Modules governed by a single Chassis Manager.
HOST Component	A physical device that is defined, in whole or part, by requirements in the HOST Standards. The HOST Components include, but are not limited to, HOST Enclosures, HOST Modules, HOST Transmission Components, and HOST External Interfaces.

Term	Definition
HOST Enclosure	A physical chassis that holds together all of the HOST Components in a Target System implementation.
HOST External Interface	Physical connection between the HOST Transmission Components and the external system.
HOST Gatekeeper	A government program office which utilizes open hardware subject matter expertise and is responsible for reviewing the Verification Authority output and controlling HOST Registration.
HOST Mezzanine Module	A HOST Component that contains functionality as defined by the HOST Resources and a physical form factor that conforms to the requirements of this HOST Tier 2 OpenVPX Standard for mezzanines.
HOST Module	A HOST Component that is a standardized element of a given implementation technology. For this Tier 2 Standard, it is defined as a VPX plug-in card, VITA 62 power supply, XMC, or PMC that has been designed to fulfill the requirements of the HOST Tier 2 OpenVPX Standard.
HOST OpenVPX Verification Methods	HOVM is a companion document that details the verification method information required for Tier 3 Specifications that conform to the requirements of the Tier 2 Standards document.
HOST Plug-In Module	A HOST Component that contains functionality as defined by the HOST Resources and plugs directly into a backplane.
HOST Ready Module	A component which was designed and developed in accordance with HOST Tier 2 Standard requirements and intended to be a HOST Module. This component has not been verified to a HOST Conformant Tier 3 Specification.
HOST Ready Module Specification	A component specification which is developed in accordance with HOST Tier 2 Standard requirements and the tenets of the Tier 3 Specification Guide.
HOST Ready Tier 3 Specification	A document adhering to the definition of a Tier 3 Specification prior to being verified and registered.
HOST Registration	The process of listing HOST Conformant Tier 3 Specifications and HOST Modules in a public listing known as the HOST Registry.
HOST Registry	A single centralized database which contains all HOST Conformant Tier 3 Specifications and Modules.

Term	Definition
HOST Verification	The act of determining whether a given module or Tier 3 Specification is HOST Conformant. For a module, this process includes various assessments to ascertain whether a module fulfills all requirements of a HOST Conformant Tier 3 Specification prior to Verification Authority involvement. For a Tier 3 Specification, this involves requirements traces from the relevant HOST Tier 2 Standard and Target System or Platform requirements prior to Verification Authority involvement.
Inspection	Inspection is an element of verification that involves an examination of the item/system or drawing form. Drawing forms are any controlled document that defines the product configuration for design, assembly, or Test. Inspection may include gauging or measurement.
Integrator	An organization responsible for bringing together HOST components into a system and ensuring they function together to meet platform requirements.
Interoperability	The ability for HOST Components to be able to connect to and communicate with one another using the same standardized interfaces and protocols.
Module Conformance Verification Process	The process to verify modules are conformant to a particular HOST Conformant Tier 3 specification.
Module Manufacturer	An organization responsible for designing, developing, and fabricating a Printed Circuit Board (PCB) intended to be utilized as a HOST Module.
Intelligent Platform Management Bus	Name for the architecture, protocol, and implementation of a special bus that interconnects the baseboard and chassis electronics and provides a communications media for system platform management information. It is defined by the Intelligent Platform Management Interface Specification (IPMI).
Module Profile	A physical mapping of ports onto a given Module's backplane Connectors and protocol mapping(s), as appropriate, to the assigned Port(s). This definition provides a first-order check of operating compatibility between Modules and slots as well as between multiple Modules in an Enclosure. Module Profiles achieve the physical mapping of ports to backplane connectors by specifying a Slot Profile. Multiple Module Profiles can specify the same Slot Profile.
Platform	A vehicle or weapons system on which a HOST based system will be installed (e.g. an aircraft).
Power Supply Resource	PSRs transform Target System power into chassis power that is supplied to HOST Modules via the system power distribution Interface. Modules that implement PSRs must support the Power Distribution Interface since that is the exclusive power distribution interface for HOST Modules.

Term	Definition
Requirements Verification Matrix	The RVM lists verification methods for both the HOST and performance (all platform derived requirements) requirements for the Tier 3 component being defined.
Slot Profile	A physical mapping of ports onto a given slot's backplane connectors. These definitions are often made in terms of Pipes. Slot Profiles also give the mapping of Ports onto Plug-In Module's backplane connectors. Unlike Module Profiles, a Slot Profile never specifies protocols for any of the defined Ports.
System Communications Transmission Interface	The SCTI carries general communications data between resources. General communications data consists of resource coordination and data messages required for general computing performance. The SCTI does not carry Platform I/O signals between resources. The SCTI can share a physical transmission medium with other Transmission Interfaces but it remains logically distinct based upon the type of data that it carries. The SCTI can be implemented as an address mapped parallel bus, a packet-switched network, or any number of other communications methods.
System I/O Transmission Interface	The SIOTI connects I/O signals between the EIOTI and I/O resources. The SIOTI does not carry general communications data between resources (i.e. data allocated to the SCTI).
System Power Distribution Interface	The SPDI distributes power from the Power Supply modules within the PSR to all modules requiring power. The power specifications and transmission methods are specific to a Tier 2 core technology standard.
Test	Test is an element of verification designed to provide data on functional features, performance, or equipment operation under fully controlled and traceable conditions. Tests generally use special instrumentation or test equipment to obtain accurate quantitative data for Analysis. The data is used to evaluate quantitative characteristics. Testing implicitly requires Analysis of the resulting test data.
Target System	A HOST based aggregation of components/modules intended to carry out a defined function on a Platform (e.g. a mission computer).
Tier 3 Conformance Verification Process	The Tier 3 Conformance Verification process is a six step process that recommends verification activities to be done on a Tier 3 document. Further details can be found in the HOST Tier 3 Verification Assessment (HOST000019-01).

Term	Definition
Tier 3 Specification	A formatted document specifying a set of requirements traced to a HOST Tier 2 Standard, Target System, or Platform that must be fulfilled for a Module to be HOST Conformant. A Tier 3 Specification contains requirements from a specific Target System and/or Platform. The format and contents of a Tier 3 Specification are elaborated on in the Tier 3 Specification Guide.
Verification Authority	An entity that reviews the results and artifacts of the Tier 3 Specification Verification and HOST Module Verification to a Tier 3 Specification.

7 Acronyms

ATCA – Advanced Telecommunications Computing Architecture

ChMC – Chassis Manager Controller

CMTI – Chassis Management Transmission Interface

COTS – Commercial-Off-the-Shelf

CVAM – Conformance Verification and Applicability Matrix

EIOTI – External I/O Transmission Interface

FP – Fat Pipe

FR – Functional Resource

FRU – Field Replaceable Unit

HOST – Hardware Open System Technologies

HOVM – HOST OpenVPX Verification Methods

IPMB – Intelligent Platform Management Bus

IPMC – Intelligent Platform Management Controller

IPMI – Intelligent Platform Management Interface

JTAG – Joint Test Action Group

OEM – Original Equipment Manufacturer

OFP – Operational Flight Program

PCI – Peripheral Component Interconnect

PCIe – Peripheral Component Interconnect Express

PMC – PCI Mezzanine Card

PSM – Power Supply Module

PSR – Power Supply Resource

PWB – Printed Wiring Board

RVM – Requirements Verification Matrix

SATA – Serial Advanced Technology Attachment

SCTI – System Communications Transmission Interface

SDR – Sensor Data Record

SEL – System Event Log

SIOTI – System I/O Transmission Interface

SMI – System Manager Interface

SPDI – System Power Distribution Interface

UD – User Defined

UTC – Coordinated Universal Time

UTP – Ultra Thin Pipe

VA – Verification Authority

XMC – Switched Mezzanine Card